

# PROJECTION TELEVISION

## HITACHI DP-2X CHASSIS TRAINING

2002 and 2003  
MODEL RELEASE

DIGITAL  
HD READY PTV



Chassis	Model #	Aspect
DP-27	51SWX20B	16X9
	57SWX20B	
	65SWX20B	
DP-27D	57TWX20B	16X9
	65TWX20B	
DP-26	65XWX20B	16X9
	57XWX20B	
	51XWX20B	
DP-24	43FWX20B	16X9
DP-23G	57GWX20B	16X9
	51GWX20B	
DP-23K	46F500	16X9
DP-23	57UWX20B	16X9
	57F500	
	57G500	
	51UWX20B	
	51F500	
	51G500	

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# **POWER SUPPLY INFORMATION**

**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 1**

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## DP-2X +6V POWER SUPPLY REGULATION EXPLANATION

**+6V Power Supply Circuit Diagram explanation:** *The Primary Chassis Discussed is the DP-27 and DP-27D. (See DP-26, DP-27 and DP-27D +6V Regulation Circuit Diagram for details). (Also, see DP-23, DP-23G and DP-24 +6V Regulation Circuit Diagram for details). Note: Items described below for the DP-23, 23G and DP-24 are shown in brackets [ ].*

### **THIS POWER SUPPLY RUNS ALL THE TIME:**

When a Projection set is plugged into an AC outlet, it must produce a power supply to energize certain circuits. These circuits are responsible for monitoring the Infrared input or Front control Keys as well as the Auxiliary inputs if the Auto Link feature is active.

These power supplies are generally labeled as Always power supplies or Standby power supplies. As an example **A+6V** would indicate a +6V power supply that's always present. If the power supply has an Sby prefix, (example Sby +6V) this too is always present if the set is plugged into the AC outlet.

The DP-2X power supply Standby voltages are regulated by monitoring the **Control +6V** which becomes the **Sby +5V** after it is regulated by **I909**.

The **Control +6V** is generated on the Secondary of **T901** pin **10** [7]. The pulse is rectified by **D941** and filtered by **C954** and becomes a +6V Power Supply.

**REGULATION:** *Note: Items for the DP-23, 23G and DP-24 are shown in brackets [ ].*

The primary route for the **Control +6V** is to pin **3** of **I909** and output as **Sby. +5V** from pin **2**. However, the regulation route is to pin **1** of **I904**. Internally, the LED is illuminated by degrees dependant upon the **Control +6V** voltage fluctuations. The internal receiver receives this light and acts as a variable resistor from pin **4** to pin **3** ground. This action causes pin **6** of **I901** to manipulate the internal oscillator within **I901**. This in turn causes the frequency of the drive pulse delivered to the Gate of the internal SMOSFET (Switch Metal Oxide Semiconductor Field Effect Transistor) to manipulate the frequency of the pulse generated on the primary of **T901**. Pin **6** [3] of **T901** is routed to pin **1** of **I901** which is the Drain of the SMOSFET. The source is connected internally to pin **2** and then to floating ground pin **9** [6] of **T901**. The floating ground is monitored by three [two] low ohm resistors, **R908**, **R909** and **R910** [**R908**, **R909**] to hot ground. Here, the current drain of the internal SMOSFET is monitored. If this current exceeds a specific value, the voltage developed by these low ohm resistors is routed back into pin **5** which is the Over Current Protection circuit. This pin will inhibit the drive signal to the gate of the SMOSFET. As soon as the excessive current situation is eliminated, the IC will recover and continue functioning.

### **B+ GENERATION FOR THE LOW VOLTAGE POWER SUPPLY DRIVER IC:**

Vcc for the Driver IC is first generated by the AC input. This voltage is called Start Up Voltage. **I901** requires **16V DC** to operate normal. However, it will begin operation at **6.8V DC** on pin **3** of **I901**.

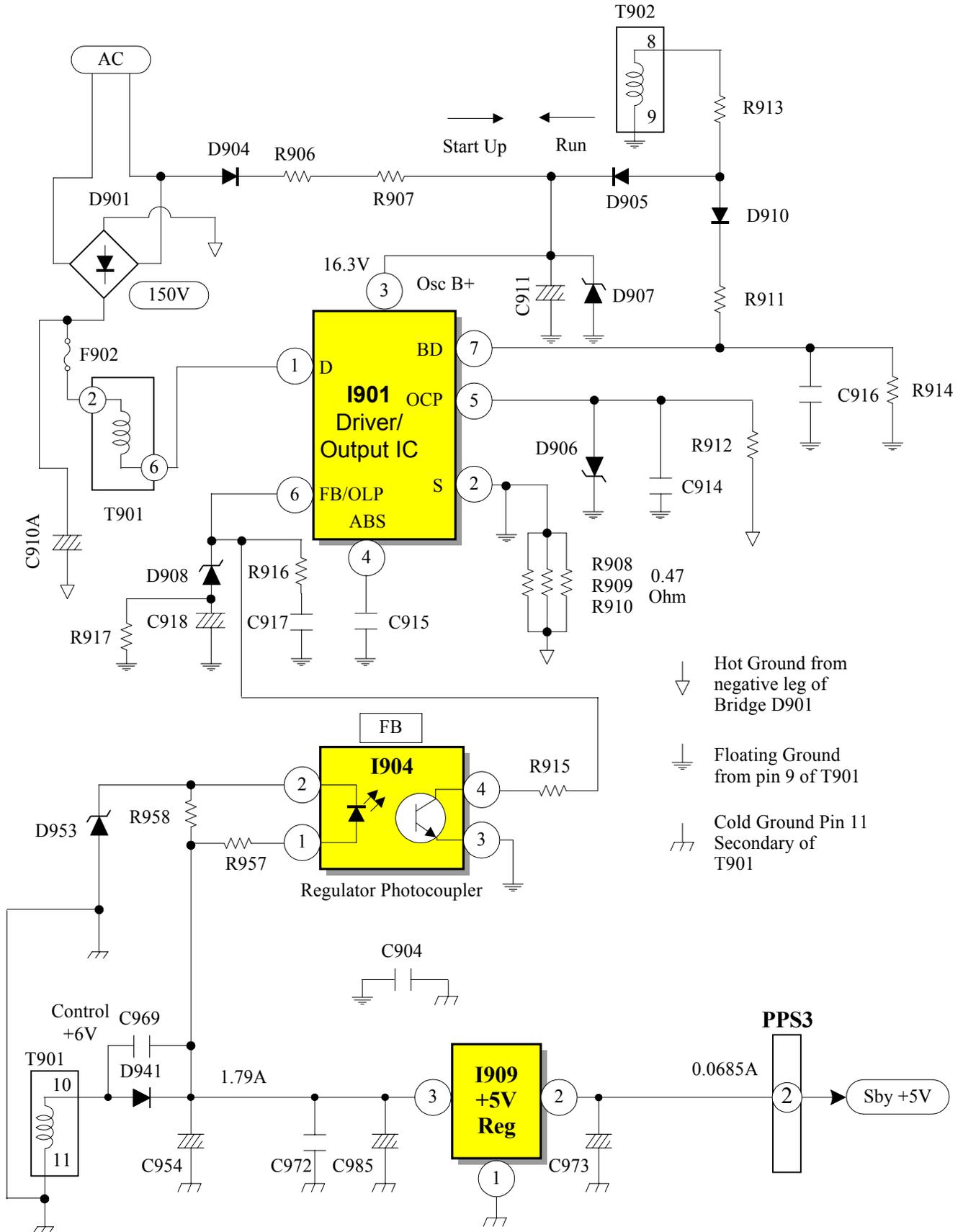
When AC is applied, AC is routed through the main fuse **F901** (a 6 Amp fuse), then through the Line filter **L901** to prevent any internal high frequency radiation for radiating back into the AC power line. After passing the filters it arrives at the main full wave bridge rectifier **D901** where it is converted to Raw 150V DC voltage to be supplied to the power supply switching transformer **T901** pin **2** [1].

However, one leg of the AC is routed to a half wave rectifier **D904** where it is rectified, routed through **R906** and **R907** (both a 68K ohm resistor), filtered by **C911**, clamped by a 30V Zener **D907** and made available to pin (3) of **I901** as start up voltage. When this voltage reaches 6.8Vdc, the internal Regulator of **I901** is turned On and begins the operation of **I901**.

When the power supply begins to operate by turning on and off the internal Switch MOS FET, the Raw 150V DC routed through **T901**, to **I901** in on pin **1** (Drain) and out on pin **2** which is the Source. The Source of the internal Switch MOS FET is routed out of pin **2** through three low ohm resistors to hot ground. When the internal Switch MOS FET turns on, it causes the transformer to saturate building up the magnet field. When the internal Switch MOS FET turns off, the magnet field collapses and the EMF is coupled over to the secondary windings, as well as the drive windings. The drive windings at pin **8** [5] of **T901** produce a run voltage pulse which is rectified by **D905**, filtered by **C911** then routed clamped by **D907** and now becomes run voltage (16V) for **I901** pin **3**.

Note too that Hot Ground is the Negative Leg of the bridge rectifier **D901** and the Floating Ground is pin **9** [6] of **T901**.

# DP-26, DP-27 and DP-27D CHASSIS POWER SUPPLY Sby +6V REGULATION Lo Voltage Power Supply





## DP-2X POWER ON RELAY CONTROLS EXPLANATION

### **Relay Controls Circuit Diagram explanation:**

*(See DP-23, DP-23G, DP-24 and DP-27, DP-27D Relay Controls Circuit Diagram for details)*

#### **POWER ON:**

When the Customer presses the Power On button on the Front control panel or the Remote control, the Microprocessor **I001** output a High from pin **59**. This high is routed to the base of **Q026** which turns this transistor On and it's collector connected to the Sty +5V line goes low. This action in turn causes the base of **Q025** to go low and turns **Q025** to turn Off. **Q025** collector is also connected to the **Sby +5V** line and it's collector pulls up to 5V.

This high is routed to the **PPS3** connector pin **4**. Provided the **Short Detection** transistor **Q903** isn't activated, (See the Lo Voltage Power Supply Shut Down Circuit for details), then the High from pin **4** is routed to the base of **Q908** turning it On.

When **Q908** turns on, it's collector is connected to the **Sby +5V** line. It's emitter pulls up and supplies a high to the base of **Q907** turning it On. When **Q907** turns on, it causes the following relays to energize.

#### **RELAYS ENERGIZED BY Q907 (DP-23, DP-23G, DP-24, DP-27 and DP-27D):**

*Note: This description refers specifically to the DP-27 and DP-27D chassis. Components identified inside brackets [ ] are for the DP-23, 23G and DP-24 chassis.*

##### **S901**

This completes the path for AC to reach the High Voltage power supply bridge diode **D902**. (See the High Voltage Regulation Circuit for details). This action starts the High Voltage power supply **SW+115V** for the deflection circuit.

##### **S902**

This completes the path for the pulse generated from pin **14 [11]** of **T901**, (+38V for DP-26, DP-27 and DP-27D) and [+29V for DP-23, DP-23G and DP-24] to reach the Audio B+ rectifier diode **D944**. Here the **Audio +38V [+29V]** is generated and output from the **PPS5** connector pins **1, 2 and 3** and on to the Audio output circuit.

##### **S903**

This completes the path for the pulse generated from pin **10 [7]** of **T901** (Control +6V), rectified by diode **D941** which produces **SW+6V** to reach the **PPS4** connector pins **7 and 6** and on to **IP52** (Switched +3.3V regulator) and **IP53** (Switched +5V regulator) on the Signal PWB.

##### **S905**

This completes the path for the pulse generated from pin **13 [10]** of **T901** (+35V) to reach the Tuning Voltage B+ rectifier diode **D943**. Here the **SW+35V** is generated and output from the **PPS3** connector pin **8** and on to the Tuners pin **9**.

#### **DP-26 ONLY: RELAYS ENERGIZED BY POWER 1 and POWER 2:**

*(See DP-26 Relay Controls Circuit Diagram for details)*

##### **Power 1: (High when the Set is turned On.)**

- When the Customer presses the Power On button on the Front control panel or the Remote control, the Microprocessor **I001** output a High from pin **59**. This high is routed to the base of **Q026** which turns this transistor On and it's collector connected to the Sty +5V line goes low. This action in turn causes the base of **Q025** to go low and turns **Q025** to turn Off. **Q025** collector is also connected to the **Sby +5V** line and it's collector pulls up to 5V.
- This high is routed to the **PPS3** connector pin **4**. Provided the **Short Detection** transistor **Q904** isn't activated, (See the Lo Voltage Power Supply Shut Down Circuit for details), then the High from pin **4** is routed to the base of **Q907** turning it On.
- When **Q907** turns on, it causes the following relays to energize.

*(Continued on page 5)*

## DP-2X POWER ON RELAY CONTROLS EXPLANATION

### RELAYS ENERGIZED BY Q907: Activated by Power \_1

- **S901**  
This completes the path for AC to reach the High Voltage power supply bridge diode **D902**. (See the High Voltage Regulation Circuit for details). This action start the High Voltage power supply **SW+115V** for the deflection circuit.
- **S902**  
This completes the path for the pulse generated from pin **14** of **T901**, (+38V) to reach the Audio B+ rectifier diode **D944**. Here the **Audio +38V** is generated and output from the **PPS5** connector pins **1, 2** and **3** and on to the Audio output circuit.
- **S903**  
This completes the path for the pulse generated from pin **10** of **T901** (Control +6V), rectified by diode **D941** which produces **SW+6V** to reach the **PPS4** connector pins **7** and **6** and on to **IP52** (Switched +3.3V regulator) and **IP53** (Switched +5V regulator) on the Signal PWB.

### **Power \_2: (High when the set is turned On and/or when the Timer is On).**

- When the Customer presses the Power On button on the Front control panel or the Remote control, the Microprocessor **I001** output a High from pin **58**. This high is routed to two different circuits.
- **DM +9V REGULATOR:**
- When Power \_2 goes high, it's routed to pin **2** of **IP01** on the Signal PWB. This is the **DM +9V** regulator and it turns on. Input to pin **5** is the **DM +10V**, **IP01** regulates this down to 9V and output it from pin **3** to the Digital Module (ATSC Tuner) pin **12** PMS1.
- The DM +9V is also routed to the Terminal PWB pin **21** of the **PST2** connector. This turns on the Selector IC **IX01** and the Monitor Out Circuit.
- Power \_2 is also routed to the **PPS3** connector pin **4** and then to the Power Supply. This high is routed to the base of **Q909** turning it On.
- When **Q909** turns on, it causes the following relays to energize.

### RELAYS ENERGIZED BY Q909: Activated by Power \_2

- **S905**  
This completes the path for the pulse generated from pin **13** of **T901** (+35V) to reach the Tuning Voltage B+ rectifier diode **D943**. Here the **SW+35V** is generated and output from the **PPS3** connector pin **8** and on to the Tuners pin **9**. This voltage is also routed out the PPS7 connector pin **6** **DM +28V**, to become tuning voltage for the Digital Tuner (ATSC) via pin **1** of the **PMS2** connector.
- **S906**  
This completes the path for the pulse generated from pin **17** (Digital Module +10V) of **T901** to reach the rectifier diode **D945**. Here the **DM +10V** is generated and output from the **PPS7** connector pin **2** and **3** and on to the DM +9V regulator **IP01**. Input to pin **5**, **IP01** regulates this down to +9V and outputs it from pin **3** to the Digital Module (ATSC Tuner) pin **12** of the **PMS1** connector.

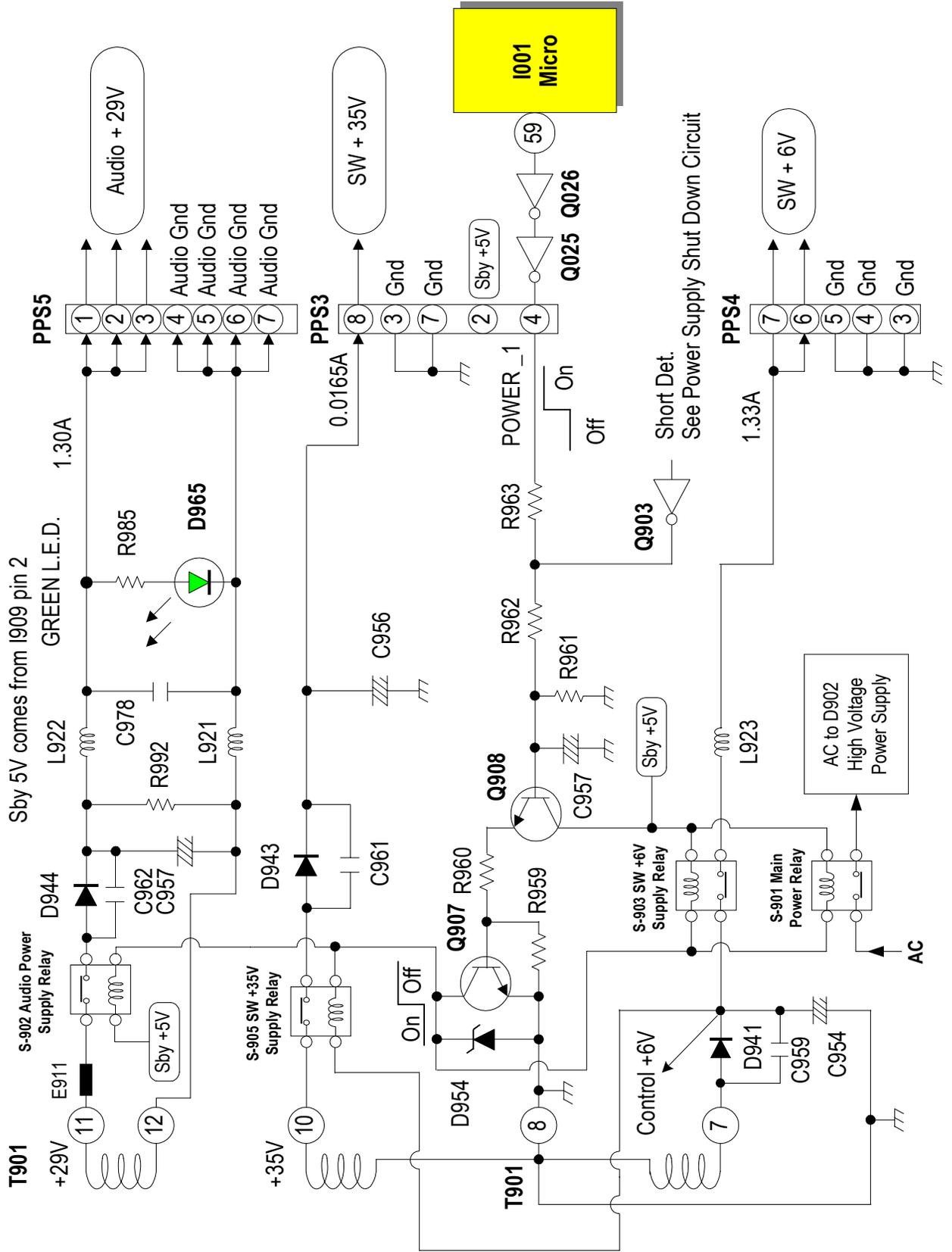
### **TIMER (Unattended Recording) OPERATION:**

**NOTE:** Power \_2 is also high when the Timer is set for unattended recordings. When the Timer is activated, the Tuners, Selector IC and Monitor output become active. During this time, **Power\_1** remains Low. This way, the Selector IC, Tuners, Audio Circuit and Monitor outputs remain active.

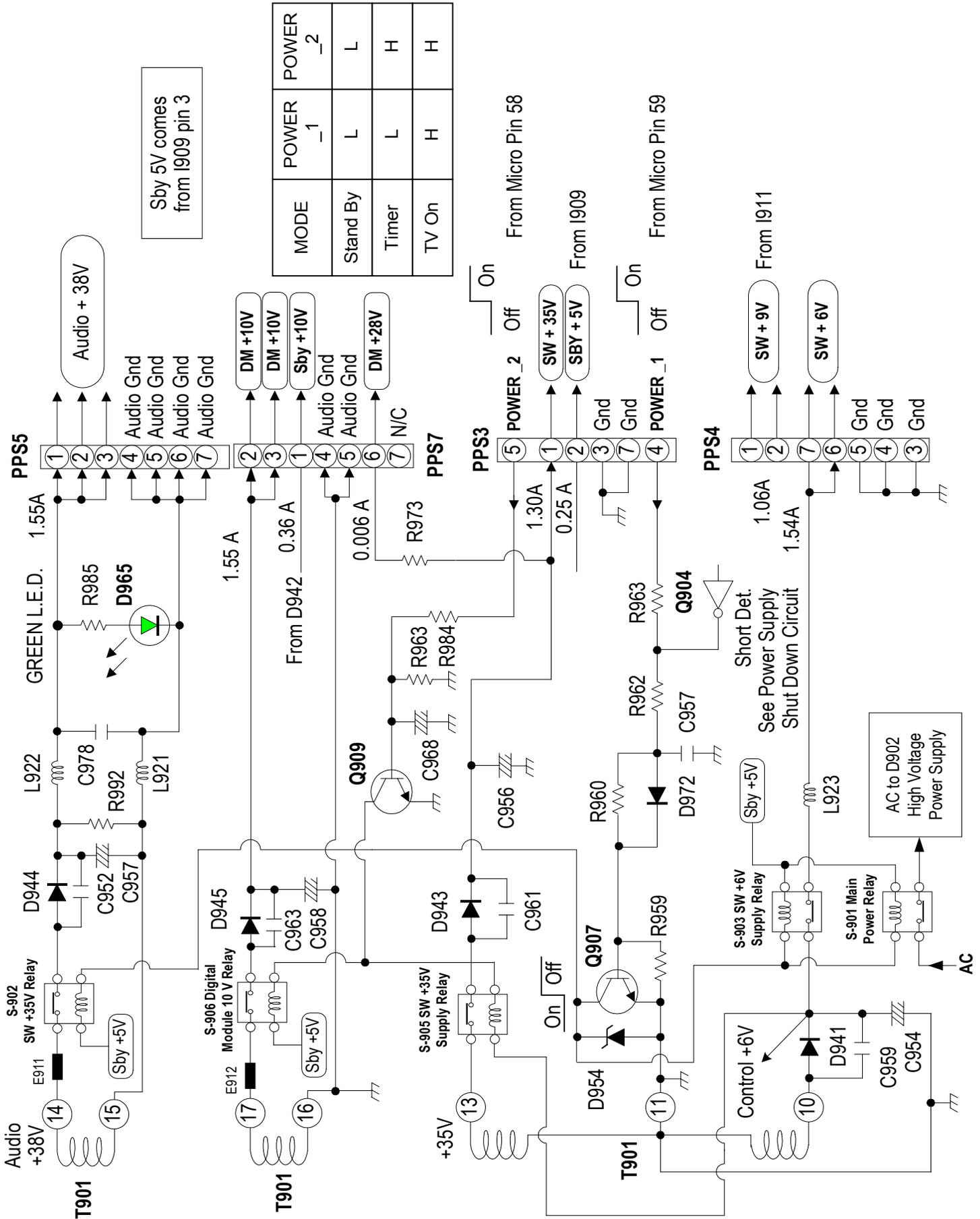
The Table below shows the logic state of Power \_1 and Power \_2.

MODE	POWER _1	POWER _2
Stand By	L	L
Timer	L	H
Power ON	H	H

# DP-23, DP-23G and DP-24 Chassis Power On Relay Controls



# DP-26 RELAY CONTROLS



Sby 5V comes from I909 pin 3



## DP-2X LOW VOLTAGE POWER SHUT DOWN EXPLANATION

### Low Voltage Power Supply Shut Down Circuit Diagram explanation:

(See DP-27 Signal Power Supply (Low Voltage) Shut-Down Circuit Diagram for details)

The Low Voltage power supply is centered around the Switching Transformer **T901** and **I901**.

This power supply creates the Standby voltages **SBY +5V** which runs anytime the set is plugged into an AC outlet. It also creates other voltages that are Switched on when the Set is turned on.

Audio +38V

SW +35V

SW +9V

SW +HVcc

The following explanation will describe the Low Voltage Power Supply Shut Down Circuit.

### POWER SUPPLY SHUTDOWN PHOTO COUPLER I905 EXPLANATION

This chassis utilizes **I901** as the Osc.\Driver \Switch for the Low Voltage power supply, just as the previous chassis have done. The Shutdown circuit, (*cold ground side detection*), removes **I901 B+** at pin **3** via the following circuit, **I905** (*the Photo Coupler*), which isolates the Hot ground from the Cold ground and couples the Shutdown signal to the Hot Ground side, **Q902** on the hot ground side and **Q901** which latches **Q902** on. When **Q902** is on, it removes B+ from pin **(3)** of **I901** (*the Vin pin*).

The Power Supply utilizes a Shutdown circuit that can trigger **Q902** from **2** input sources. (**1** of these Short Detection circuits are not operational in Stand By mode). **I905** is activated by a Low being applied to pin **2**, which forward biases the internal LED. The light from this internal LED is then coupled to the receiver transistor. The receiver transistor turns On and output a High from pin **3**. This high is routed to the base of **Q902** turning it On, which grounds out the Vin at pin **(3)** of **I901**, disabling the power supply. **Q901** will keep a high on the base of **Q902** as long as there is any voltage available at its Emitter.

The individual Shut Down circuits will be discussed later.

### GENERAL INFORMATION:

All of the Power Supply Shutdown circuitry can be broken down into the following category;

- **Voltage Missing Detection or Short Detection**
- **Voltage Too High Detection**
- **Excessive Current Detection**
- **Negative Voltage Loss Detection**

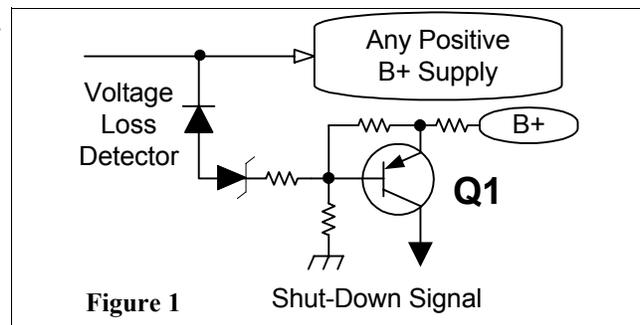
The following will explain all of these commonly used circuits. The Service Technician should become familiar with the appearance of these circuit and their function.

### **VOLTAGE LOSS or SHORT DETECTION**

(See Figure 1)

One circuit used is the **Voltage Loss Detection** circuit. This is a very simple circuit that detects a loss of a particular power supply and supplies a Pull-Down path for the base of a PNP transistor.

This circuit consist of a diode connected by its cathode to a positive B+ power supply. Under normal conditions, the diode is reversed biases, which keeps the base of **Q1** pulled up, forcing it OFF. However, if there is a short or excessive load on the B+ line that's being monitored, the diode in effect will have a LOW on its cathode, turning it ON. This will allow a current path for the base bias of **Q1**, which will turn it ON and generates a Shutdown Signal.



(Continued on page 10)

## DP-2X LOW VOLTAGE POWER SHUT DOWN EXPLANATION

### VOLTAGE TOO HIGH DETECTION

(See Figure 2)

Another circuit used is the **Voltage Too High Detection** circuit. In the example shown in Figure 2, the zener diode **D1** is connected to a voltage divider. If the voltage source rises too high, the voltage at the divider center point will rise as well and trigger or fire the zener diode which produces a Shutdown signal.

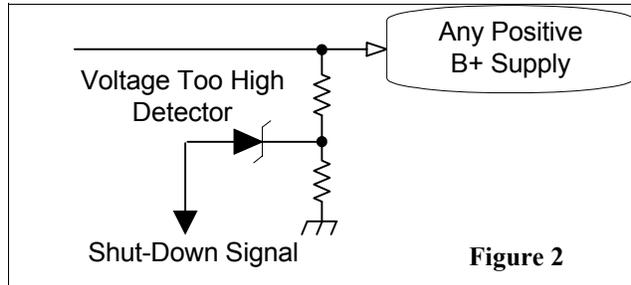


Figure 2

### EXCESSIVE CURRENT DETECTION

(See Figure 3)

One very common circuit used in many Hitachi television products is the B+ **Excessive Current Sensing** circuit. In this circuit is a low ohm resistor in series with the particular power supply, (labeled B+ in the drawing). The value of this resistor is determined by the maximum current allowable within a particular power supply. In the case of Figure 1, the value is shown as a **0.47 ohm**, however it could be any low ohm value. When the current demand increases, the voltage drop across the resistor increases. If the voltage drop is sufficient to reduce the voltage on the base of the transistor, the transistor will conduct, producing a Shutdown signal that is directed to the appropriate circuit.

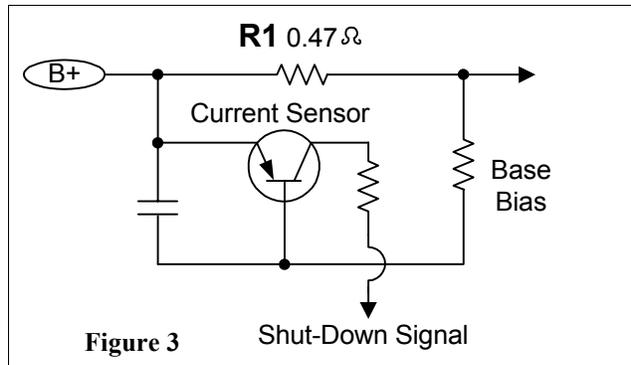


Figure 3

### NEGATIVE VOLTAGE LOSS DETECTION

(See Figure 4)

The purpose of the Negative Voltage Loss detection circuit is to compare the negative voltage with its' counter part positive voltage. If at any time, the negative voltage drops or disappears, the circuit will produce a Shutdown signal.

In Figure 5, there are two resistors of equal value. One to the positive voltage, (shown here as +12V) and one to the negative voltage, (shown here as -12V). At their tie point, (neutral point), the voltage is effectually zero (0) volts. If however, the negative voltage is lost due to an excessive load or defective negative voltage regulator, the neutral point will go positive. This in turn will cause the zener diode to fire, creating a Shutdown Signal.

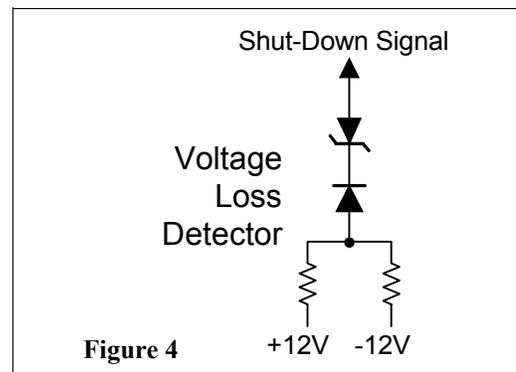


Figure 4

### SPECIFIC INFORMATION:

In addition, there are 7 Hot Ground side Shutdown inputs that are specifically detected by the main power driver IC **I901**. These sensors circuits protect **I901** from excessive current, temperature or over voltage.

### HOT GROUND SIDE SHUT DOWN SENSING CIRCUITS. (Specific to I901).

**LATCHED SHUT DOWN MONITORS:** (AC must be removed to recover).

1. (OVP) **Pin 3** is monitored for Over Voltage Protection at pin 3 of **I901**.
2. (TSD) **I901** itself is monitored for Excessive Heat. This block is labeled TSD. (Thermal Sensing Device).
3. (OLP) Over Load Protection monitors the difference between the Hot Ground and Floating Ground.

**RECOVERING SHUT DOWN INPUT:** (Driver IC will recover on it's own when trouble is removed.)

4. (OCP) **Pin 5** monitors the low ohm resistors, **R908, R909, and R910**. If these resistors have an excessive

(Continued on page 11)

## DP-2X LOW VOLTAGE POWER SHUT DOWN EXPLANATION

current condition caused by monitoring the current through the internal Switch MOS FET, the voltage will rise and pin 5 has an internal Over Voltage detection op-amp. If this voltage rises enough to trigger this op-amp, the IC will stop producing a drive signal.

5. (ABS) **Pin 4** also has **C915** monitoring spike current in case the CRTs “Snap” indicating a quick discharge of High Voltage.
6. (BD) **Pin 7** Monitors the Run Voltage generated by pin **18** of **T901** for excessive voltage.

### COLD GROUND SIDE SHUT DOWN SENSING CIRCUITS. (AC must be removed to recover).

*(See DP-27 Signal Power Supply (Low Voltage) Shut-Down Circuit Diagram for details)*

Looking at Pin **2** of **I905** the shut down events are triggered by two routes.

#### **D963, D962:**

The cathode of **D963** is connected through **R982** to pin **10** of **PPS3**. This in turn is connected to **R298** which is connected directly to the **3.3V** power supply produced by **IP81** on the Signal PWB. If something were to load this line down, **D963** would forward bias and supply a current path for pin **2** of **I905**. This in turn would produce a Shut Down event. *See Power Supply Shutdown Photo Coupler I905 Explanation on the previous page.*

#### **Q910:**

This transistor's base is connected to **Q911** through **D955**. **Q911** emitter is connected to **Q912**. This transistor is the Shut down enable circuit.

#### **DP-27 SHUT DOWN CIRCUIT:**

There are a total of **3** individual Shutdown inputs to the photo coupler **I905**.

There are a total of **3** individual Shutdown inputs to the Relay Inhibit transistor **Q903** from the power supply.

There are a total of **4** individual Shutdown inputs to the Relay Inhibit transistor **Q903** from the Deflection Circuit. For a total of **10** individual Shutdown inputs that will kill the Lo Voltage Power Supply. *(Note: The Hi Voltage Power Supply Shutdown will be discussed later.)*

All of the Cold Ground side Shutdown detection circuits can be categorized by the two previously described circuits

In the following explanation, the Shutdown circuits will be grouped. This will assist the Service Technician with trouble shooting the Chassis, by understanding these circuits and having the associated circuit routs, the technician can then “*Divide and Conquer*”.

#### **Voltage Loss Detection through I905 Photo coupler**

- Shorted STBY +3.3V generated by **IP81** and monitored by (**R298**) on Signal PWB through **PPS3** pin **10** to (**D963**) on Low Voltage Power Supply PWB. Labeled **PROT-SBY** on the Schematic.
- Shorted SW+2.2V (**IP52** pin **5**) on Signal PWB monitored by **RP53** through **PPS3** pin **11** to to (**D961**) on Low Voltage Power Supply PWB. Labeled **PROT-SW** on the Schematic.
- Shorted SW+3.3V (**IP52** pin **2**) on Signal PWB monitored by **DP53**, **RP53** through **PPS3** pin **11** to to (**D961**) on Low Voltage Power Supply PWB. Labeled **PROT-SW** on the Schematic.
- Shorted SW+5V (**IP53** pin **2**) on Signal PWB monitored by **DP54**, **RP53** through **PPS3** pin **11** to to (**D961**) on Low Voltage Power Supply PWB. Labeled **PROT-SW** on the Schematic.

#### **Q903 Relay Inhibit Activation.**

*From the Power Supply.*

##### **SW +115V Voltage Too High Detection**

- Monitored by (**D927**) *See additional Shut Down Circuit Diagram for details.*

##### **SW +115V Excessive Current Detection**

- Monitored by (**Q905**) *See additional Shut Down Circuit Diagram for details*

*(Continued on page 12)*

## DP-2X LOW VOLTAGE POWER SHUT DOWN EXPLANATION

### SW -28V Loss Detection

- Monitored by (D937) See additional Shut Down Circuit Diagram for details

### From the Deflection Circuit PPD3 connector pin 6.

#### Vertical B+ 28V Voltage Excessive Current Detection

- Monitored by (Q604) See Deflection Protect Power Supply Shutdown Diagram for details.

#### Excessive High Voltage Detection

- Monitored by (DH15) See Deflection Protect Power Supply Shutdown Diagram for details.

#### -5V Loss Detection

- Monitored by (DK90) See Deflection Protect Power Supply Shutdown Diagram for details.

#### Side Pincushion Failure Detection

- Monitored by (D702, D703) See Deflection Protect Power Supply Shutdown Diagram for details

If any one of these circuits activate the base of Q903 will go High and remove the Power On High from PPS3 connector pin 4 and the power supply will STOP.

### SOME SHUTDOWN CIRCUITS ARE DEFEATED IN STANDBY MODE. (Set Off).

As indicated in the Power Supply (Lo Voltage) Shutdown circuit diagram, 3 of the shut down inputs are not active when the set is in standby.

- Shorted SW+2.2V (IP52 pin 5) on Signal PWB monitored by RP53 through PPS3 pin 11 to (D961) on Low Voltage Power Supply PWB. Labeled PROT-SW on the Schematic.
- Shorted SW+3.3V (IP52 pin 2) on Signal PWB monitored by DP53, RP53 through PPS3 pin 11 to (D961) on Low Voltage Power Supply PWB. Labeled PROT-SW on the Schematic.
- Shorted SW+5V (IP53 pin 2) on Signal PWB monitored by DP54, RP53 through PPS3 pin 11 to (D961) on Low Voltage Power Supply PWB. Labeled PROT-SW on the Schematic.

These voltage loss sensing circuits are defeated because the SW (Switched) power supplies are turned off in standby. So to prevent faults triggering of the shutdown circuit, the sensing circuits are turned off also..

Q911 supplies the high for shutdown if any of the voltage loss circuits become activated. Q911 requires emitter voltage to operate. Emitter voltage is supplied from the emitter of Q912. Q912s base is connected to the power on/off line. When the set is not on or turned off, the power on/off line goes Low. This Low pulls the cathode of D956 low, removing the base voltage of Q912 turning it OFF. This removes the emitter voltage from Q911 and this circuit can not function. The base of Q912 is also connected to the SW +6V line. This voltage must be active for this circuit to function.

### B+ GENERATION FOR THE LOW VOLTAGE POWER SUPPLY DRIVER IC:

Vcc for the Driver IC is first generated by the AC input. This voltage is called Start Up Voltage. I901 requires 16V DC to operate normal. However, it will begin operation at 6.8V DC on pin (3) of I901.

When AC is applied, AC is routed through the main fuse F901 (a 6 Amp fuse), then through the Line filter L901 to prevent any internal high frequency radiation for radiating back into the AC power line. After passing the filters it arrives at the main full wave bridge rectifier D901 where it is converted to Raw 150V DC voltage to be supplied to the power supply switching transformer T901 pin (2).

However, one leg of the AC is routed to a half wave rectifier D904 where it is rectified, routed through R906 and R907 (both a 68K ohm resistor), filtered by C911, clamped by a 30V Zener D907 and made available to pin (3) of I901 as start up voltage. When this voltage reaches 6.8Vdc, the internal Regulator of I901 is turned On and begins the operation of I901.

When the power supply begins to operate by turning on and off the internal Switch MOS FET, the Raw 150V DC routed through T901, in on pin 1 (Drain) and out on pin 2 which is the Source. The Source of the internal Switch MOS FET is routed out of pin (2) through three low ohm resistors to hot ground. When the internal Switch MOS FET turns on, it causes the transformer to saturate building up the magnet field. When the internal Switch MOS FET turns off, the magnet field collapses and the EMF is coupled over to the secondary windings, as well as the drive windings. The drive windings at pin (8) produce a run voltage pulse which is rectified by D905, filtered by C911 then routed clamped by D907 and now becomes run voltage (16V) for I901 pin 3.



## DP-2X SW +115V POWER SUPPLY REGULATION EXPLANATION

### Hi-Voltage Power Supply Circuit Diagram explanation:

*(See DP-27 Chassis Power Supply SW+115V Regulation Circuit Diagram for details)*

**THIS POWER SUPPLY RUNS ONLY WHEN THE SET IS TURNED ON:**

### TURNING ON THE SW +115V POWER SUPPLY:

When the Set is turned on, the Microprocessor **I001** Outputs a Power On command via pin **59**. This Power On command is routed through **Q025** and **Q026** to the **PPS3** connector pin **4**. This High will be passed to the base of **Q908** provided the Short Detection Shut Down sensor **Q903** isn't activated. When the base of **Q908** goes high, it's emitter will go high and drive the base of **Q907** high turning it on. This will supply a ground path for the power on Relay **S901** turning it on. When the relay is energized, AC is supplied to the Bridge rectifier **D902**. *See Relay Controls on the Power Supply for details.*

This rectifier develops raw 150V which is routed through **F903** to Pins **1** and **2** of **T902**. This voltage is routed through the primary coil inside **T902** and out pins **5** and **6** to pin **3** of **I902** which is the Drain of the internal Switch MOS FET. The Ground return path for the primary voltage is out pin **2** of **I902** which is the Source of the internal Switch MOS FET and then through three low ohm resistors **R926**, **R927** and **R928**. *See SW+115V Regulation Circuit Diagram for details.*

### SW +115 REGULATION

SW +115V pulse is generated from pin **11** of **T902**. This pulse is rectified by **D915**, filtered by **C927** and then routed through the Excessive Current sensing circuit **R941** and **Q905**.

The primary route for the SW +115V is through **E907**, **L914** to pin **9** and **10** of **PPD6** and output as SW +115V to the Deflection Circuit.

However, the regulation route is through **E906** to pin **1** of **I907**. Internally, the regulator transistor works as a variable resistor whose resistance is dependant upon the SW +115V voltage fluctuations. The internal variable resistor manipulates the current flow from pin **2** to pin **3** ground. This will cause the voltage at pin **2** of **I906** to be manipulated. Internally, the LED is illuminated by degrees dependant upon the SW +115V voltage fluctuations. The internal receiver receives this light and acts as a variable resistor from pin **4** to pin **3** which is the regulation control signal.

This action causes pin **1** of **I902** to manipulate the internal oscillator within **I902**. This in turn causes the frequency of the drive pulse delivered to the Gate of the internal SMOSFET (Switch Metal Oxide Semiconductor Field Effect Transistor) to manipulate the frequency of the pulse generated on the primary of **T902**. The current drain of the internal SMOSFET is monitored by the three low ohm resistors mentioned above. If this current exceeds a specific value, the voltage developed by these low ohm resistors is routed back into pin **1** which is the Over Current Protection circuit as well as the Regulation Control pin. This pin will inhibit the drive signal to the gate of the SMOSFET. As soon as the excessive current situation is eliminated, the IC will recover and continue functioning.

### B+ GENERATION FOR THE HIGH VOLTAGE POWER SUPPLY DRIVER IC:

Vcc for the Driver IC is first generated by the AC input. This voltage is called Start Up Voltage. **I902** requires **16V DC** to operate normal. However, it will begin operation at **6.8V DC** on pin **4** of **I902**.

When AC is applied to the main full wave bridge rectifier **D902** where it is converted to Raw 150V DC voltage to be supplied to the power supply switching transformer **T902** pin **1** and **2**.

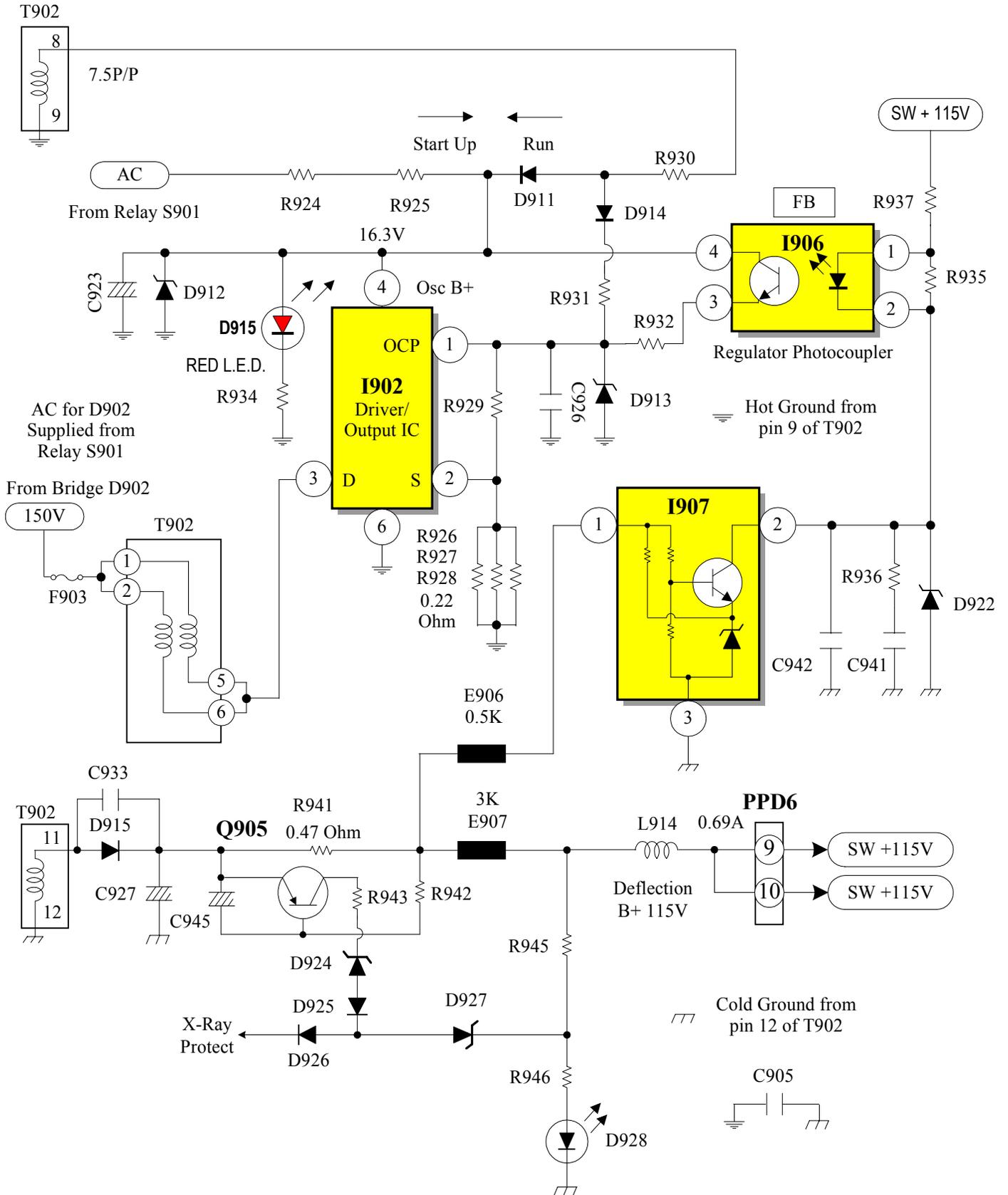
However, one leg of the AC is routed to a half wave rectifier consisting of **R924** and **R925** (both a 3.9K ohm resistor), filtered by **C923**, clamped by a 36V Zener **D912** and made available to pin **4** of **I902** as start up voltage.

When this voltage reaches 6.8Vdc, the internal Regulator of **I902** is turned On and begins the operation of **I902**.

When the power supply begins to operate by turning on and off the internal Switch MOS FET, the Raw 150V DC routed through **T902**, in on pin **1** (Drain) and out on pin **2** which is the Source. The Source of the internal Switch MOS FET is routed out of pin **(2)** through three low ohm resistors to hot ground. When the internal Switch MOS FET turns on, it causes the transformer to saturate building up the magnet field. When the internal Switch MOS FET turns off, the magnet field collapses and the EMF is coupled over to the secondary windings, as well as the drive windings. The drive windings at pin **(8)** produce a run voltage pulse which is rectified by **D911**, filtered by **C923** then routed clamped by **D912** and now becomes run voltage (**16V**) for **I902** pin **4**.

The RED LED **D915** can be used to determine if the B+ to I902 is present or not.

# DP-2X CHASSIS POWER SUPPLY SW +115V REGULATION High Voltage Power Supply



## DP-2X ADDITIONAL SHUTDOWN CIRCUITS EXPLANATION

### Additional Power Supply Shut Down Circuit Diagram explanation:

(See DP-27 Additional Power Supply Shut Down Diagram for details)

Use this explanation and Diagram in conjunction with the following diagrams.

DP-2X Signal Power Supply (Low Voltage) Shut Down Circuit (Continuation A)

The following circuits are routed to the Lo Voltage Shut Down Circuit through connection point (A) depicted on the Circuit drawing:

### **SW +115V EXCESSIVE CURRENT DETECTION**

(See Figure 1)

One very common circuit used in many Hitachi television products is the B+ **Excessive Current Sensing** circuit. In this circuit is a low ohm resistor in series with the SW +115V. The value of this resistor **0.47 ohm**. When the current demand increases, the voltage drop across the resistor increases. If the voltage drop is sufficient to reduce the voltage on the base of **Q905**, the transistor will conduct, producing a Shut-down signal that is directed to the appropriate circuit indicated on the drawing as point (A).

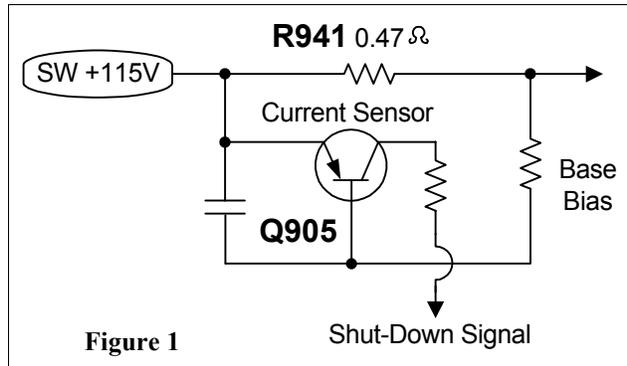


Figure 1

### **NEGATIVE VOLTAGE LOSS DETECTION**

(See Figure 2)

The purpose of the Negative Voltage Loss detection circuit is to compare the negative voltage with its' counter part positive voltage. If at any time, the negative voltage drops or disappears, the circuit will produce a Shutdown signal.

In Figure 2, there are two resistors of equal value, (15K). One to the positive voltage SW +28V and one to the negative voltage SW -28V. At their tie point, (*neutral point*), the voltage is effectually zero (0) volts. If however, the negative voltage is lost, the neutral point will go positive. This in turn will cause the zener diode D937 to fire, creating a Shutdown Signal through **D936** and on to the appropriate circuit indicated on the drawing as point (A).

Note: The LED **D940** used for visual trouble shooting is illuminated by the current draw from +28V to the -28V supply.

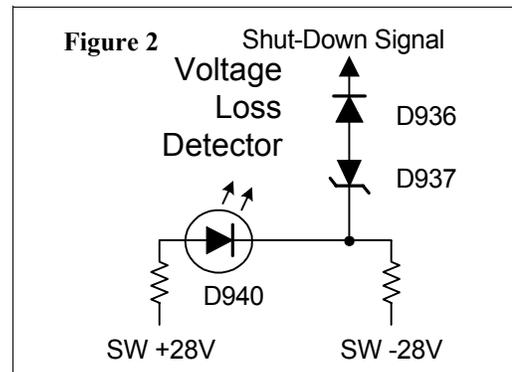


Figure 2

### **VOLTAGE TOO HIGH DETECTION**

(See Figure 3)

Another circuit used is the **Voltage Too High Detection** circuit. In the example shown in Figure 3, the zener diode **D927** is connected to a voltage divider. If the voltage source rises too high, the voltage at the divider center point will rise as well and trigger or fire the zener diode which produces a Shutdown signal through **D926** and on to the appropriate circuit indicated on the drawing as point (A).

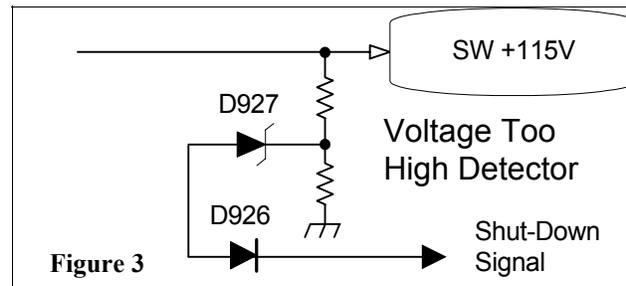
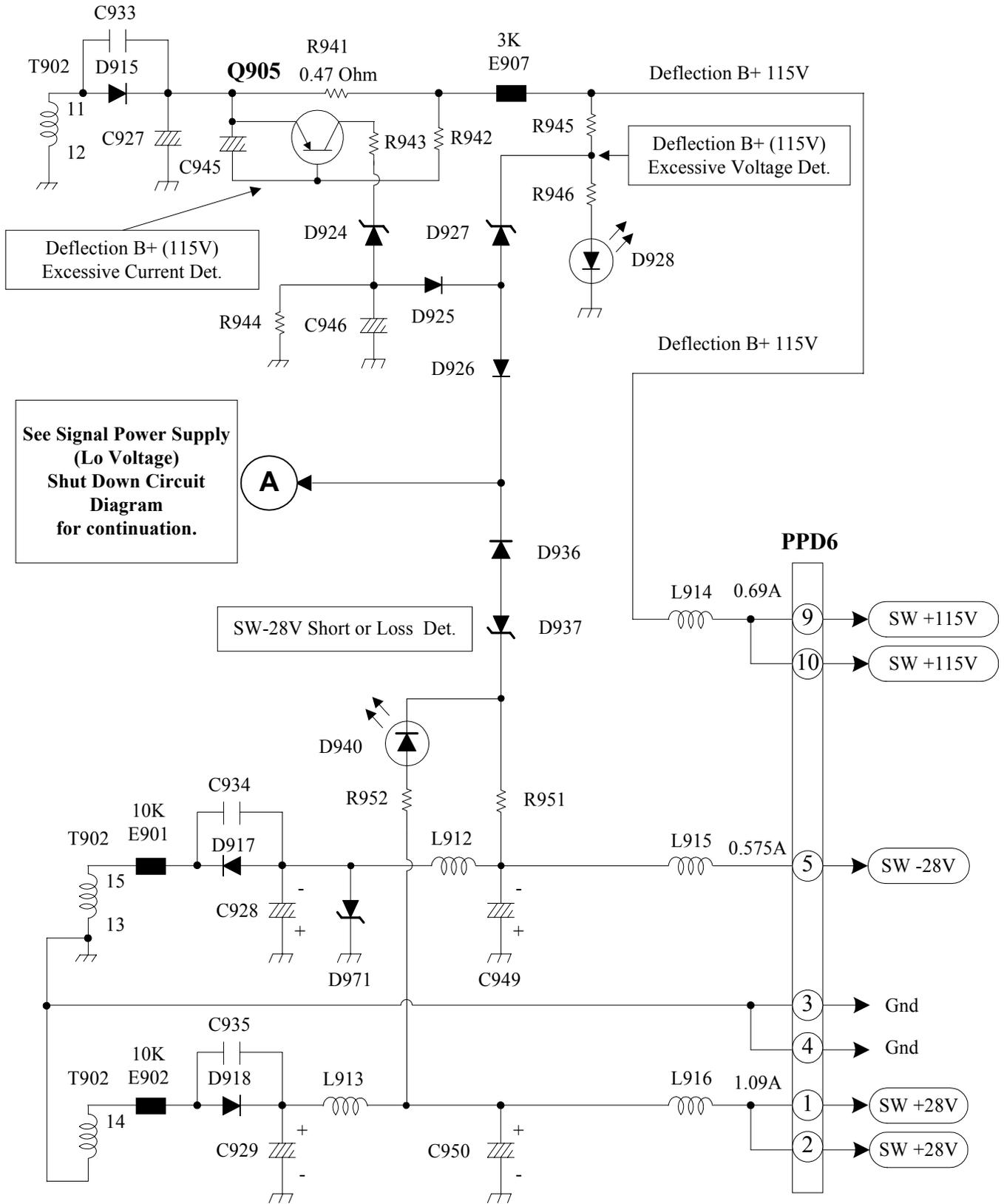


Figure 3

# DP-2X ADDITIONAL POWER SUPPLY SHUT DOWN DIAGRAM



## DP-2X PROTECT SHUTDOWN CIRCUIT EXPLANATION

### Protect Shut Down Circuit Diagram explanation:

(See DP-27 Protect Shut Down Diagram for details)

Use this explanation and Diagram in conjunction with the following diagram, DP-2X Signal Power Supply (Low Voltage) Shut Down Circuit (PROTECT\_DEF)

The following circuits are routed to the Lo Voltage Shut Down Circuit through connection point (PROTECT\_DEF) depicted on the Circuit drawing:

### **EXCESSIVE HIGH VOLTAGE DETECTION**

Whenever the High Voltage fluctuates, every other pin off the flyback will fluctuate as well. In this case, a lower voltage source can be used to determine the status of the High Voltage.

Pin 5 (50P) is used to monitor for excessive High Voltage. The pulse off the flyback is rectified by **DH13** and filtered by **CH17**. This voltage sets on the cathode of two zener diodes **DH15** and **DH14**.

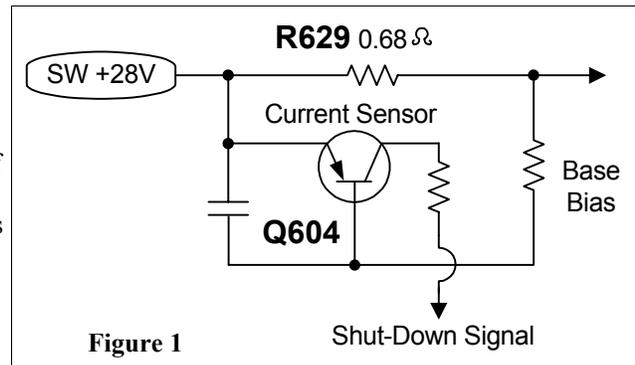
**DH15** is a HZ22V zener. If the voltage at the cathode rises too high, the zener will fire and send a Shut Down signal through **PPD3** pin 6. This signal is routed to the appropriate circuit on the Lo Voltage Shut Down Circuit. The Shut Down signal is depicted as **PROTECT\_DEF**.

**DH14** is a HZ36V zener. If the voltage at the cathode rises too high, the zener will fire and send a Shut Down signal through to pin 7 of **IH01** which is the OVP input pin. This high will cause **IH01** to stop producing the Hi Voltage Drive signal from pin 1.

### **EXCESSIVE CURRENT TO THE VERTICAL OUTPUT IC DETECTION**

(See Figure 1)

This circuit uses a low ohm resistor **R629** in series with the SW +28V. The value of this resistor **0.68 ohm**. When the current demand increases, the voltage drop across the resistor increases. If the voltage drop is sufficient to reduce the voltage on the base of **Q604**, the transistor will conduct, producing a Shut-down signal through **D608** through **PPD3** pin 6. This signal is routed to the appropriate circuit on the Lo Voltage Shut Down Circuit. The Shut Down signal is depicted as **PROTECT\_DEF**.

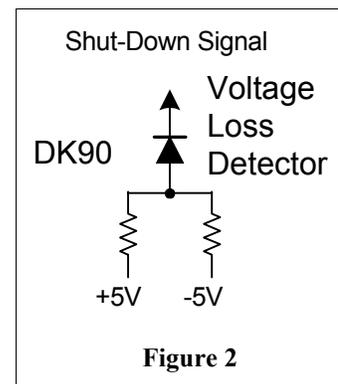


### **SIDE PINCUSHION FAILURE DETECTION**

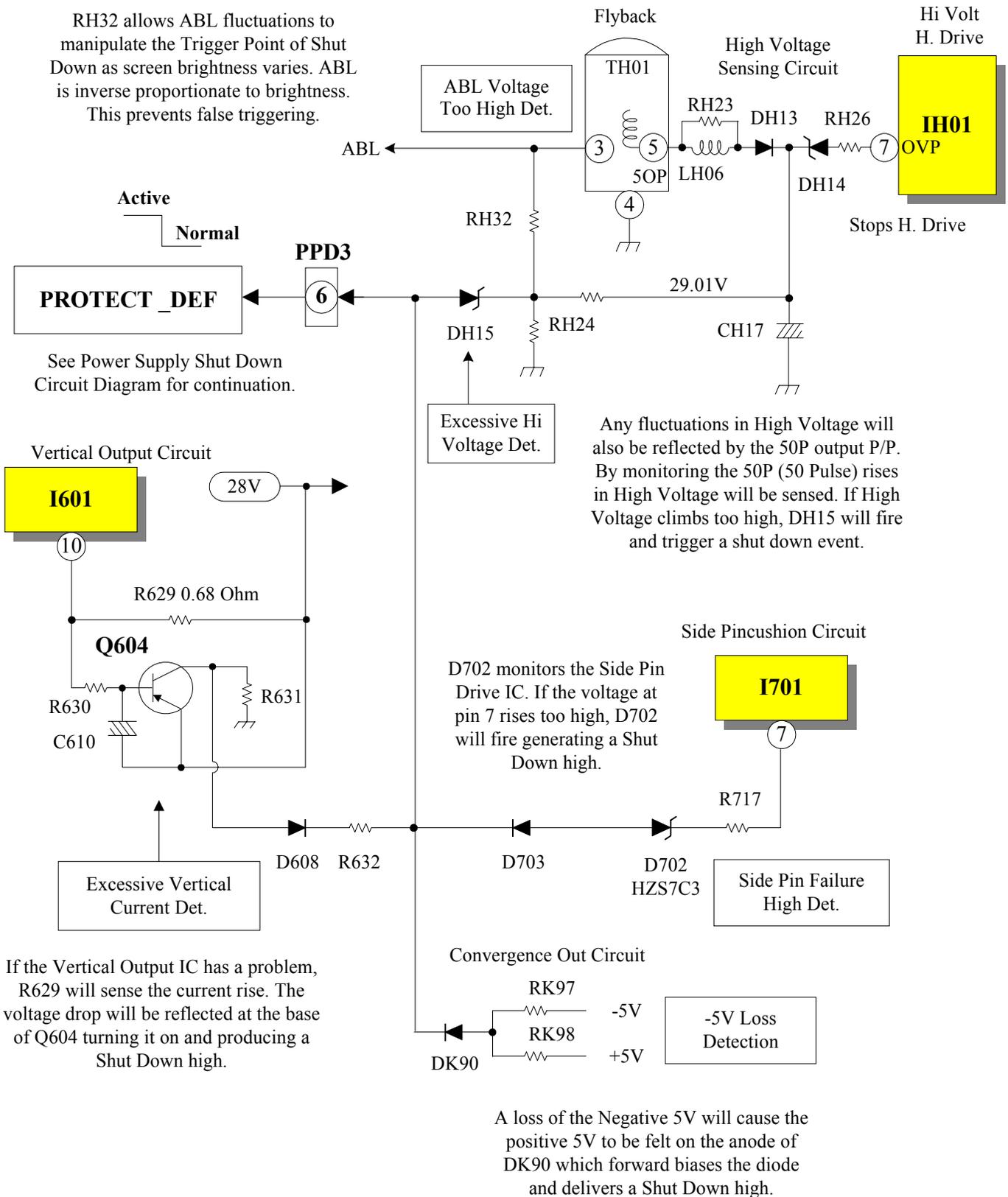
If the side pincushion circuit fails in such a way as to produce an excessive high on the cathode of **D702** (a HZS7C3) the zener will fire producing a Shutdown signal through **D703** through **PPD3** pin 6. This signal is routed to the appropriate circuit on the Lo Voltage Shut Down Circuit. The Shut Down signal is depicted as **PROTECT\_DEF**.

### **-5V LOSS DETECTION**

The purpose of the Negative Voltage Loss detection circuit is to compare the negative voltage with its' counter part positive voltage. If at any time, the negative voltage drops or disappears, the circuit will produce a Shutdown signal. In Figure 2, there are two resistors of equal value. One to the positive voltage +5V and one to the negative voltage -5V). At their tie point, (*neutral point*), the voltage is effectually zero (0) volts. If the negative voltage is lost, the neutral point will go positive. This high is routed through **DK90** through **PPD3** pin 6. This signal is routed to the appropriate circuit on the Lo Voltage Shut Down Circuit. The Shut Down signal is depicted as **PROTECT\_DEF**.



# DP-2X DEFLECTION PROTECT POWER SUPPLY SHUTDOWN DIAGRAM



## DP-2X LED (Visual Trouble Detection) CIRCUIT EXPLANATION

### **LED Used for Visual Trouble Shooting Circuit Diagram explanation:**

*(See DP-2X LED (Visual Trouble Detection) Diodes Signal Power Supply Diagram for details)*

#### **5 LEDs, 4 GREEN AND 1 RED**

In the DP-2X chassis, there are 5 total LEDs that can be used for Visual Trouble shooting. 4 Green and 1 Red. Use these LEDs to determine if the set is experiencing a problem.

The LEDs can be used in the following ways.

#### **OFF:**

- If the LED is off, then the power supply that is being monitored is unavailable. (Excluding the possibility that the LED itself is malfunctioning). NOTE: If **D940** LED opens, then the set will be in shut down condition because of it's current flow explained below.
- If the LED turns on but then quickly goes off before the others, then the power supply that is being monitored can be suspected.

#### **RED LED D915**

**D915** is used to monitor the Start Up and Run voltage for the Driver IC **I902**. This IC is used to generate the following voltages.

SW +115V

220V

HEATER

SW+7V

SW-7V

SW +28V

SW -28V

This LED is attached to pin 4 of **I902**. If the voltage is missing, the LED will not light.

#### **GREEN LEDs D965, D954, D940 and D928.**

##### **D965 (Audio +38V)**

- Monitors the **Audio +38V** output from the **PPS5** connector pin 1, 2 and 3.

##### **D954 (SW +9V)**

- Monitors the **SW +9V** generated by the SW +9V regulator **I911** pin 3 output from the **PPS4** connector pin 1 and 2.

##### **D940 (SW +28V)**

- Monitors the SW +28V output from the **PPD6** connector pin 1 and 2.
- *Note: This LED requires the SW -28V power supply to be functioning to operated. If the LED opens, or the negative SW -28V is shorted, this LED will not illuminate and the set will shut down.*

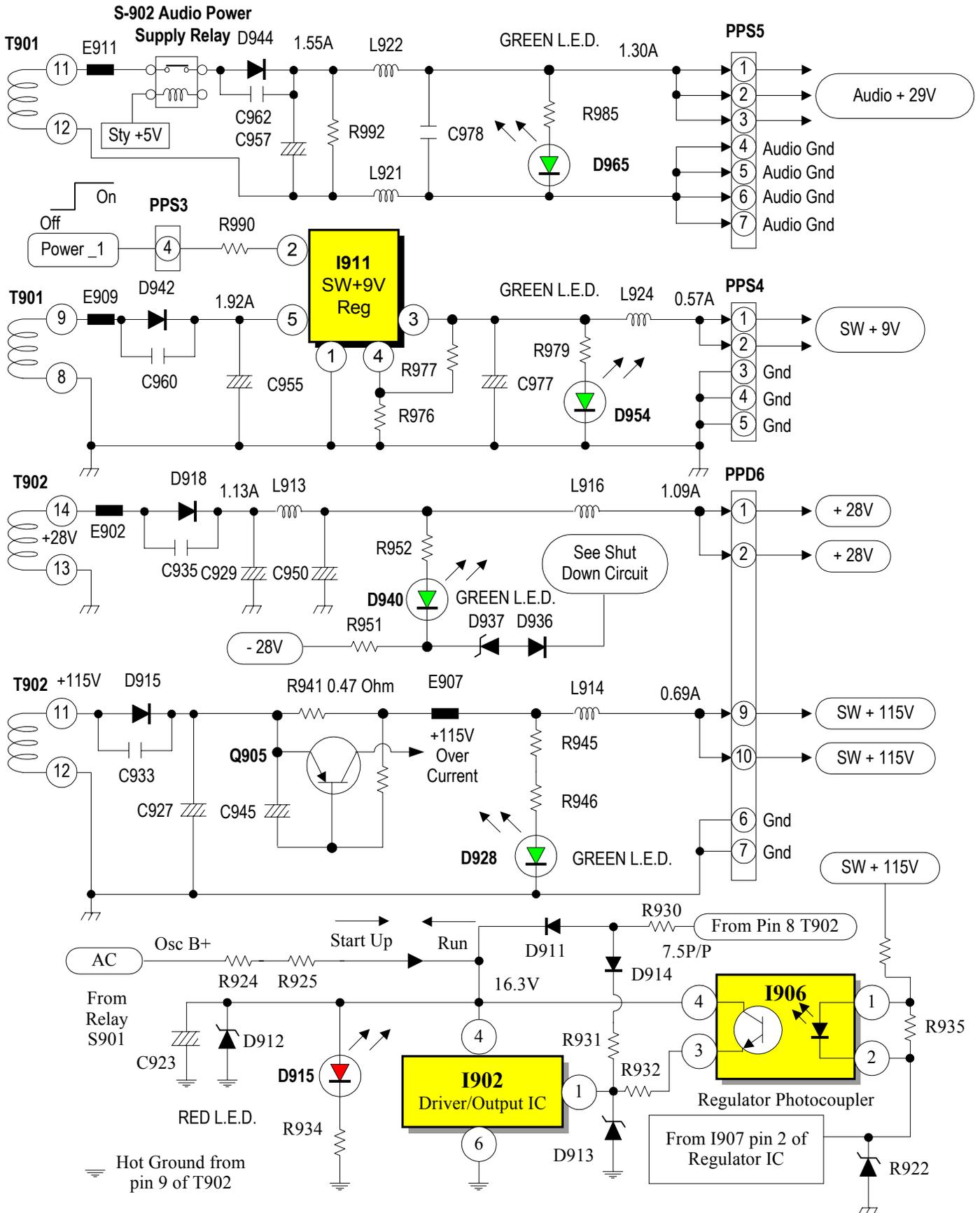
##### **D928 (SW +115V)**

- *Monitors* the SW +115V output from the **PPD6** connector pin 9 and 10.

# DP-23, DP-23G and DP-24 CHASSIS

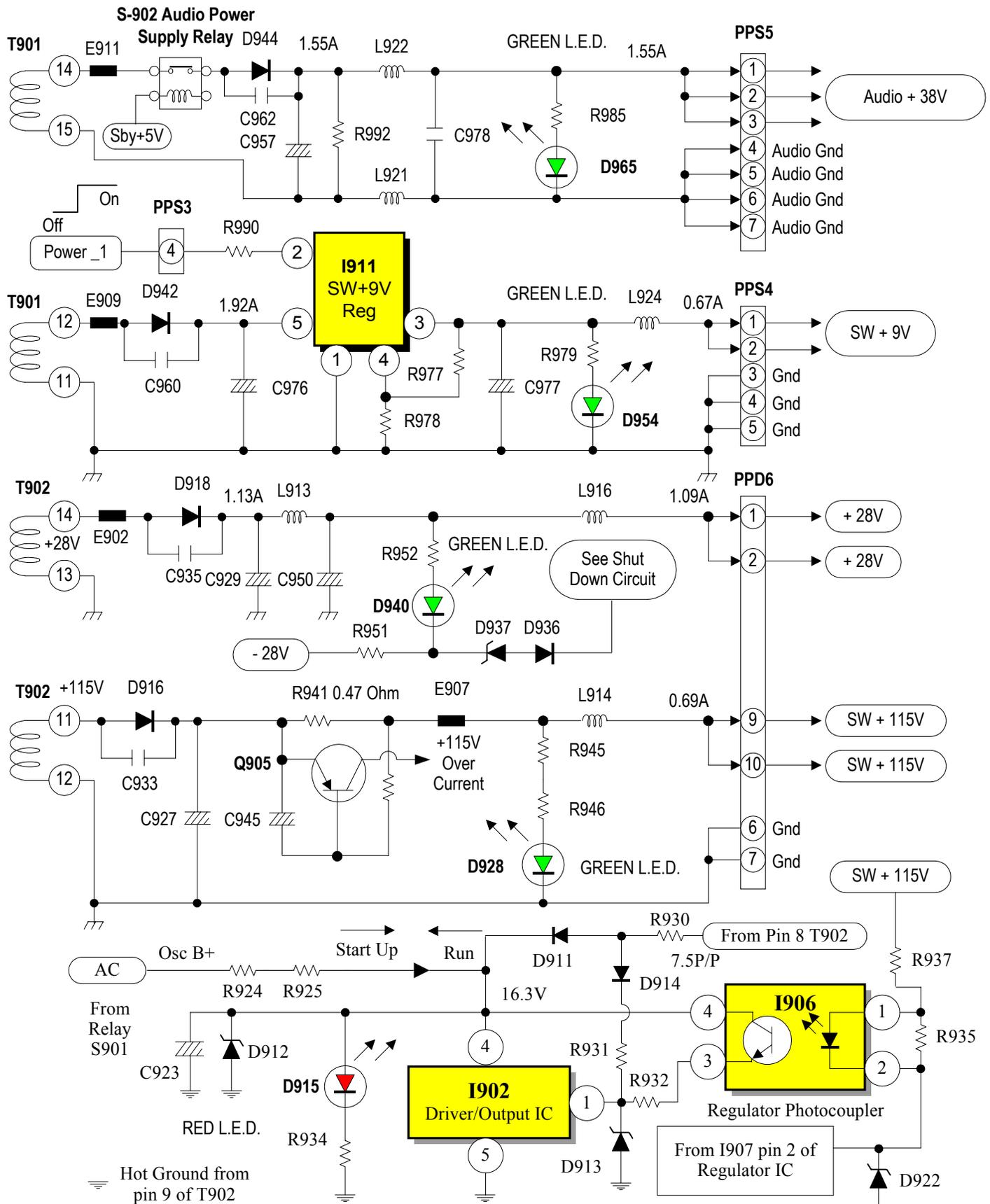
## L.E.D. (Visual Troubleshooting) Low Voltage Power Supply

### (5 Total L.E.D. for visual trouble sensing , 4 Green and 1 Red)

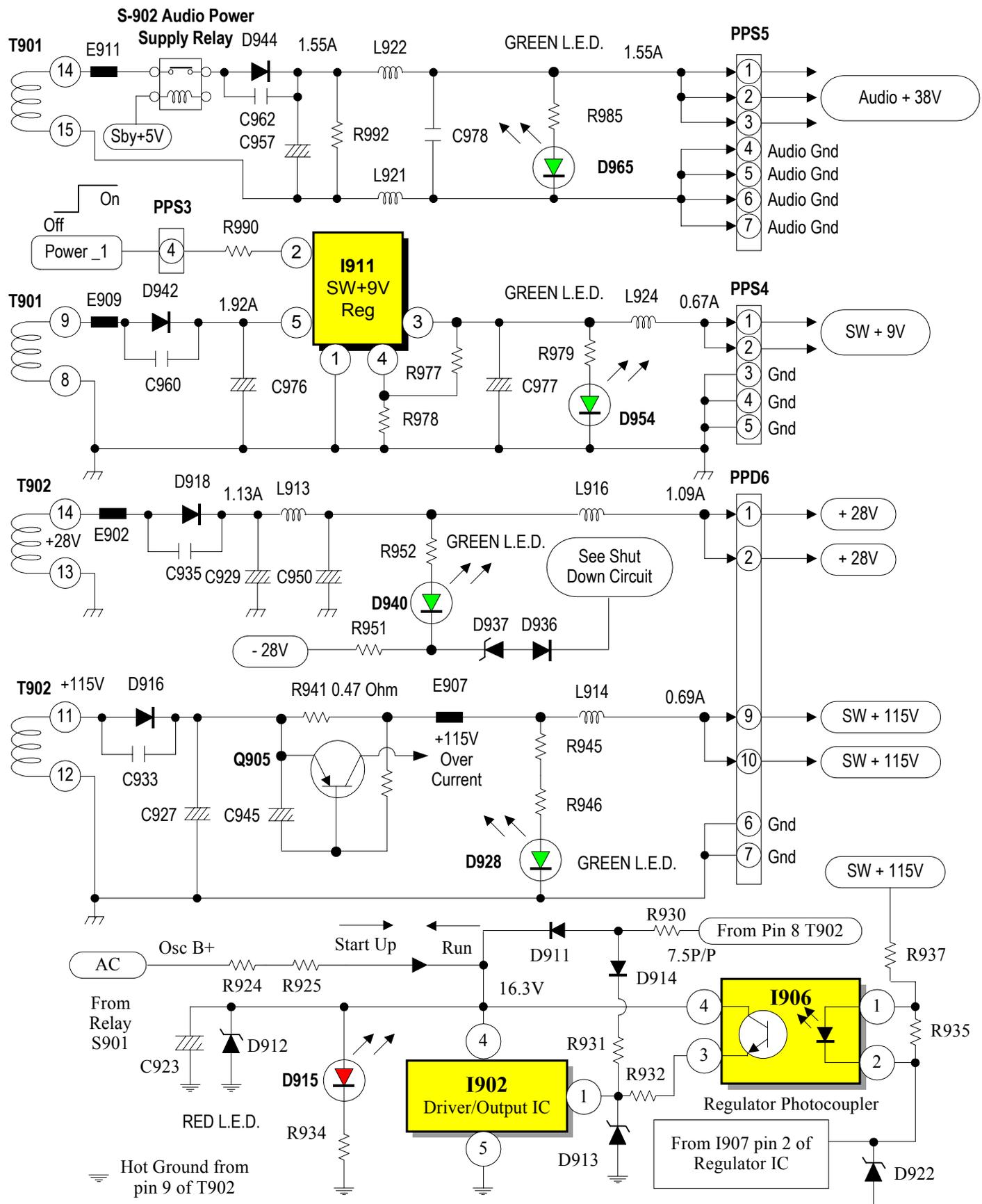


# DP-26 CHASSIS

## L.E.D. (Visual Trouble Detection) Diodes Signal Power Supply (5 Total L.E.D. for visual trouble sensing observation, 4 Green and 1 Red)



# DP-27/D CHASSIS L.E.D. (VISUAL TROUBLE DETECTION) DIODES SIGNAL POWER SUPPLY (5 Total L.E.D. for visual trouble sensing observation, 4 Green and 1 Red)



**NOTES**

# **MICROPROCESSOR INFORMATION**

## **DP-2X CHASSIS DIAGRAMS**

# **SECTION 2**

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## DP-2X MICROPROCESSOR DATA COMMUNICATIONS CIRCUIT EXPLANATION

### **PinP Tuner U302 (monaural only, but audio not used).**

The Microprocessor controls the Main Tuner by SDA2 (Data) and SCL2 (Clock) I<sup>2</sup>C communication lines. SCL2 and SDA2 lines for the Main Tuner are output from the Microprocessor at pins (31 SDA2 and 28 SCL2) respectively. These lines go directly to the Main Tuner, SDA2 at pin (5) and SCL2 at pin (4). These lines control band switching, programmable divider set-up information, pulse swallow tuning selection, etc...

### **EEPROM I003**

The EEPROM is ROM for many different functions of the Microprocessor. Channel Scan or Memory List, Customer set ups for Video, Audio, Surround etc... are memorized as well. Also, some of the Microprocessors internal sub routines have variables that are stored in the EEPROM, such as the window for Closed Caption detection. Data and Clock lines are SDA1 from pin (30) of the Microprocessor to pin (5) of the EEPROM and SCL1 from pin (29) of the Microprocessor to pin (6) of the EEPROM. Data travels in both directions on the Data line.

### **Flex Converter FC04**

The projection television is capable of displaying NTSC as well as ATSC (SDTV) including HD (High Definition). The Flex Converter is responsible for receiving any video input and converting it to 33.75 KHz output. This output is controlled by sync and by the customer's menu and how it is set up. The set up can be 4X3 or 16X9 for DTV, or letterbox. This set also has something called "16X9 Normal Mode". This bypasses the Flex Converter completely and inputs the 1080i signal directly to the Rainforest IC I401. The Flex Converter can take any NTSC, S-In, Component, NTSC or Progressive, Interlaced, 480I, 720P, 1080i signal.

Control for the Flex Converter is Clock, Data and Enable lines.

Clock, Data and Enable lines for the Flex Converter are output from the Microprocessor at pins (52 Data, 53 Clock and 55 FCENABLE). The FCENABLE line is routed through the PFC1 connector pin 12 and the FCDATA line is routed through the PFC1 connector pin 11, the FC Clock is routed through the PFC1 connector pin 10.

The Clock, Data and Enable lines must be routed through the Level Shift IC I007 to be brought up to 5V.

Clock is input to I007 at pins (2 Clock) and is output at pins (18).

Data is input to I007 at pins (4 Clock) and is output at pins (16).

Enable is input to I007 at pins (6 Clock) and is output at pins (14).

Data from the Flex Converter is also sent back to the Microprocessor. Data from the Flex is sent out of the PFC1 connector pin 11 to pin 5 of I007, level shifted down to 3.3V and output at pin 15 into pin 51 of the Microprocessor I001.

### **Level Shift I007**

The Microprocessor operates at 3.3Vdc. Most of the Circuits controlled by the Microprocessor operate at 5Vdc. The Level Shift IC steps up the DC voltage to accommodate.

- Pin 18 outputs a Clock signal, used by the Flex Converter
- Pin 14 outputs an Enable signal, used by the Flex Converter
- Pin 16 outputs a Data signal, used by the Flex Converter.
- Pin 15 outputs Data, sent from the Flex Converter

### **Rainforest I401 (Video/Chroma Processor)**

The Video Processing IC (Rainforest) is responsible for controlling video/chroma processing before the signal is made available to the CRTs. Some of the emphasis circuits are controlled by the customer's menu. As well as some of them being controlled by AI, (Artificial Intelligence).

Communication from the Microprocessor via pins (31 SDA2 and 28 SCL2) to the Rainforest IC pins (31 and 30) respectively.

### **BBE Control IA01 (Surround)**

The DP-2X chassis utilizes BBE Surround.

Communication from the Microprocessor via pins (31 SDA2 and 28 SCL2) to the BBE IC pins (13 and 14) respectively.

*(Continued on page 3)*

## **DP-2X MICROPROCESSOR DATA COMMUNICATIONS CIRCUIT EXPLANATION**

### **ON THE TERMINAL PWB: (Through the connector PST2)**

#### **A/V Selector IX01**

The A/V Selector IC is responsible for selecting the input source for the Main Picture as well as the source for the PinP or Sub picture. Communication from the Microprocessor via pins (**30 SDA1** and **29 SCL1**) to the **PST2** connector pins (**5** and **4**) respectively then to **IX01** pins (**34** and **33**) respectively.

#### **Main Video Chroma IZ02**

The Main Video Chroma IC processes the video and chroma from the 3D Y/C circuit for the main picture. It receives the Y and chroma and prepares it for the Flex Converter by outputting Y Cr/Cb (NTSC Only). Communication from the Microprocessor via pins (**31 SDA2** and **28 SCL2**) to connector **PST2** pins (**2** and **1**) then to **IZ02** pins (**13** and **14**) respectively.

#### **Sub Video Chroma IZ01 (PinP)**

The PinP Video Chroma IC processes the video and chroma from the 2 Line Comb filter circuit for the Sub picture. It receives the Y and chroma and prepares it for the Flex Converter by outputting Y Cr/Cb (NTSC Only). Communication from the Microprocessor via pins (**31 SDA2** and **28 SCL2**) to connector **PST2** pins (**2** and **1**) then to **IZ02** pins (**13** and **14**) respectively.

#### **Y Pr/Pb Selector IX02**

Any input that is not already in the Y Pr/Pb or Y Cr/Cb state, will have be converted to this state by **I501**. The Main Y Pr/Pb Selector IC selects the appropriate input between the Tuner, AV Inputs, S-Inputs or Components. Communication from the Microprocessor via pins (**31 SDA2** and **28 SCL2**) to connector **PST2** pins (**2** and **1**) to **IX04** pins (**31** and **30**) respectively.

#### **3D Y/C IW01 (IC mounted directly on the Terminal PWB).**

The 3D Y/C IC is a Luminance/Chrominance separator, as well as a 3D adder. Separation takes place digitally. Using advanced separation technology, this circuit separates using multiple lines and doesn't produce dot pattern interference or dot crawl. The 3D effect is a process of adding additional emphasis signals to the Luminance and Chrominance. These signals relate specifically to transitions. Transitions are the point where the signal goes from dark to light or vice versa. The 3D adds a little more black before the transition goes to white and a little more white just before it gets to white. It also adds a little more white just before it goes dark and a little more dark just before it arrives. This gives the impression that the signal pops out of the screen or a 3D effect.

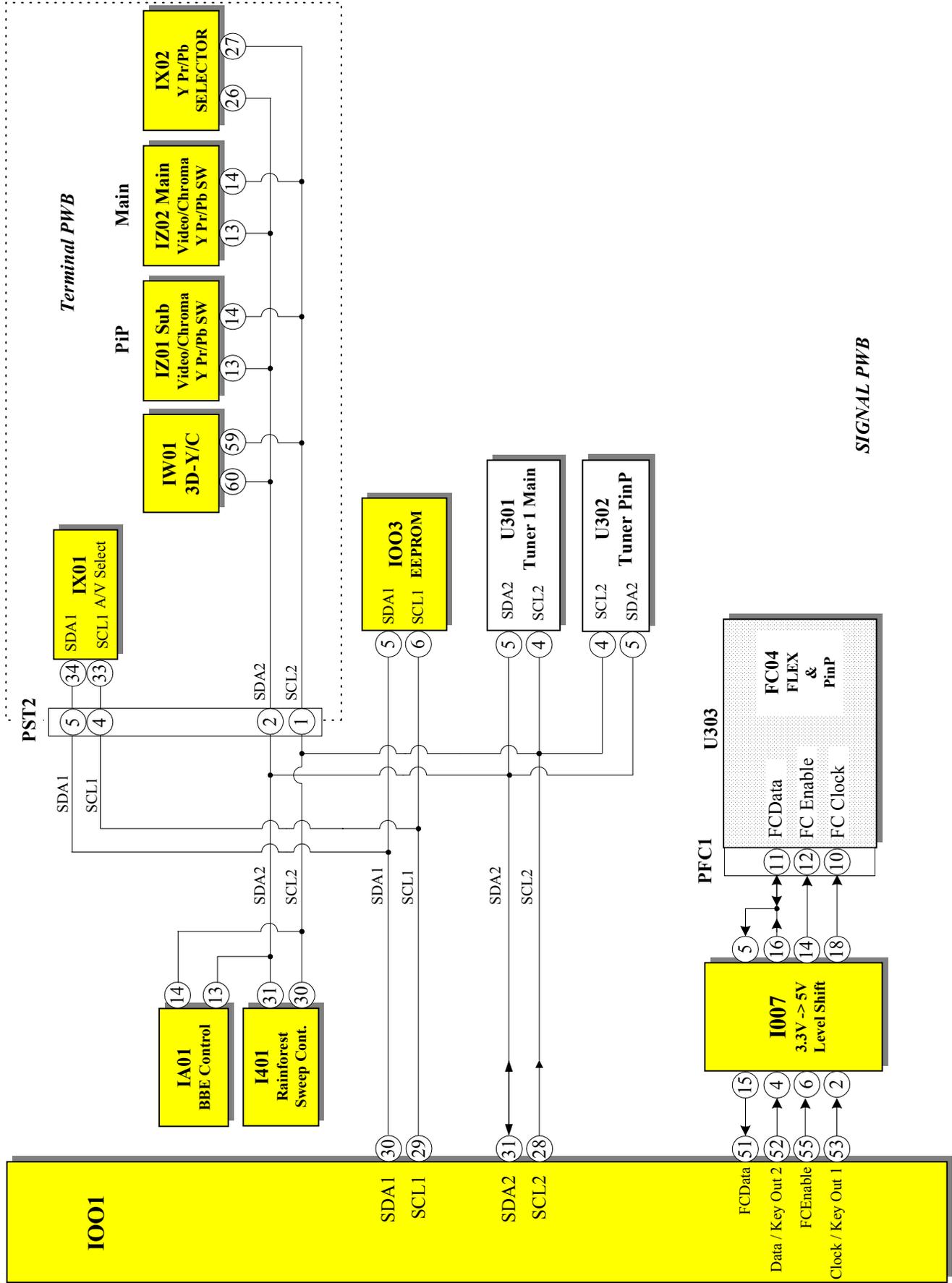
The Microprocessor communicates with the 3D Y/C IC via I<sup>2</sup>C bus data and clock. The communications ports from the Microprocessor are pins (**31 SDA2** and **28 SCL2**) to connector **PST2** pins (**2** and **1**) to the 3D Y/C **IW01** pins (**60** and **59**) respectively.

The Microprocessor also is able to turn on and off circuits within the 3D Y/C circuit determined by customer menu set-up.

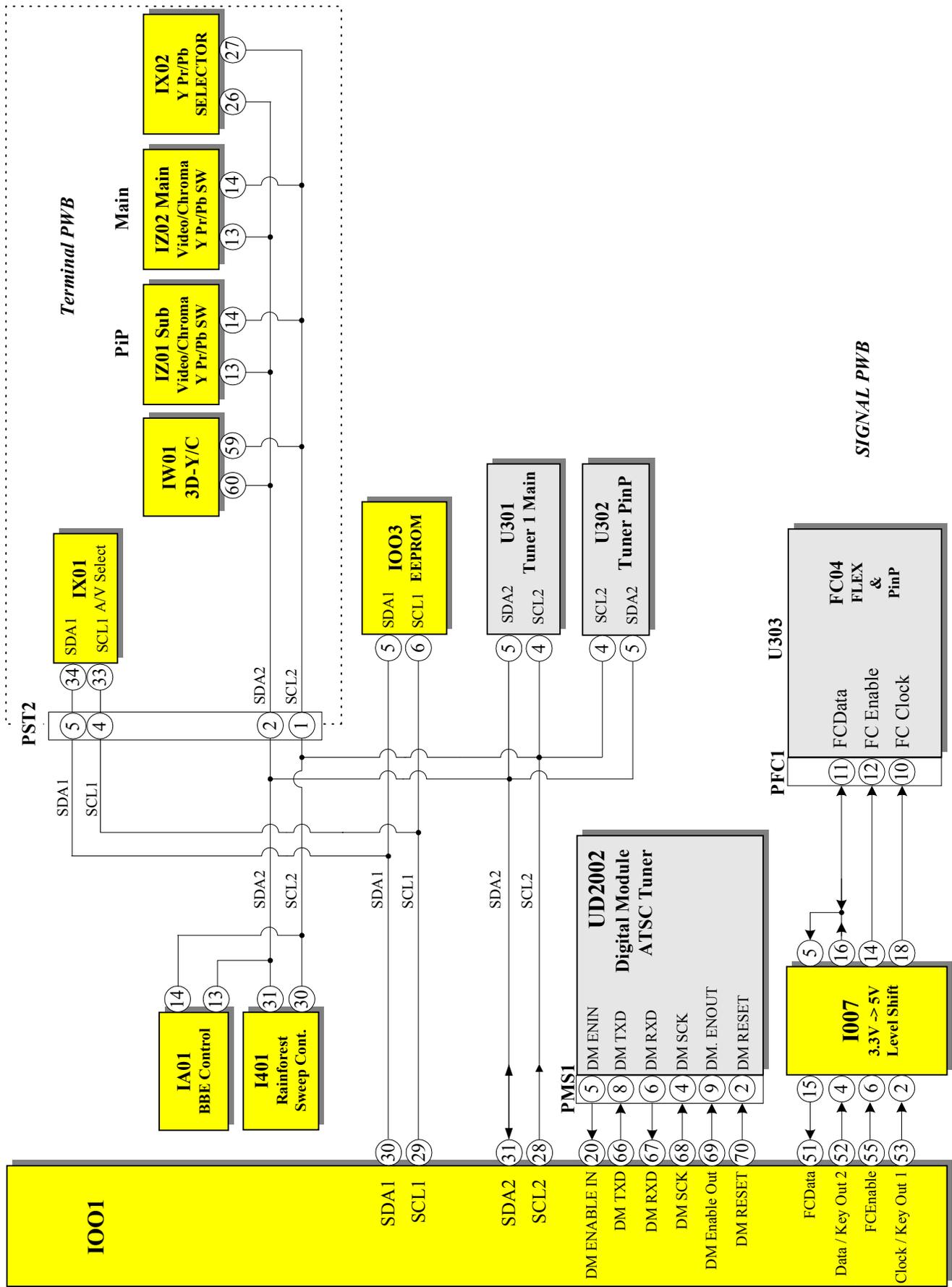
### **DP-26 MICROPROCESSOR DATA COMMUNICATIONS DIAGRAM**

The DP-26 has the addition of the Digital Module (ATSC Tuner).

DP-23, 23G, 24, 27 and 27D CHASSIS MICROPROCESSOR DATA COMMUNICATIONS CIRCUIT DIAGRAM



# DP-26 Chassis Microprocessor Data Communications



## DP-2X MICROPROCESSOR NTSC SYNC INPUT CIRCUIT EXPLANATION

### ***Microprocessor NTSC Sync circuit diagram.***

*(See DP-2X Chassis NTSC Sync to Microprocessor Signal Path Diagram for Details)*

The Microprocessor **I001** must have Sync inputs from the Chassis to Lock its generation of OSD, Closed Caption, Customer's Menu, Service Menu, etc. ....

The Chassis feeds back this information in the form of Blanking pulses and Sync from the Video. The following describes the types of feedback sync signals.

### **(62) H BLK (Horizontal Blanking):**

- H Blk is input to the Microprocessor at Pin **62**. H Blk is generated from the Deflection Transformer pulse off pin 7 of **T701**, wave shaped by **Q706**. Then routed out the **PPD2** connector pin **8** to the Power Supply. Then out the **PPS2** connector pin **8** to the Signal PWB. From here it is sent to the base of **Q024** where it gets level shifted and inverted and into pin **62** of the Microprocessor.

### **(64) V BLK (Vertical Blanking):**

- V Blk is input to the Microprocessor at Pin **64**. V Blk is generated from the Vertical Output IC **I601** pin **11**. Then routed out the **PPD2** connector pin **12** to the Power Supply. Then out the **PPS2** connector pin **12** to the Signal PWB. From here it is sent to the base of **Q023** where it gets level shifted and inverted and into pin **64** of the Microprocessor.

### **(93) MAIN AFC (Automatic Frequency Control):**

- Main AFC is input to the Microprocessor at Pin **93**. Main AFC is generated from the Main Tuner **U301** pin **16**. Then routed to **Q020** and **Q015**. Then into pin **93** of the Microprocessor.
- The Microprocessor uses this input signal to align or adjust the precise Oscillator and Programmable divider settings within the Main Tuner for proper Reception.

### **(92) SUB AFC (Automatic Frequency Control for PinP Tuner):**

- Sub AFC is input to the Microprocessor at Pin **92**. Sub AFC is generated from the Sub Tuner **U302** pin **16**. Then routed to **Q016** and **Q017**. Then into pin **92** of the Microprocessor.
- The Microprocessor uses this input signal to align or adjust the precise Oscillator and Programmable divider settings within the PinP Tuner for proper Reception.

### **(100) MAIN CCD IN:**

- The Microprocessor receives Main Sync information and strips the Closed Caption Data from line 21. This composite sync signal is supplied to the Microprocessor from **I005** pin **14**. It uses this same input for stripping V Chip Data.
- When an NTSC component input is supplied to Input **2**, this is called 480i. This must also be monitored for Closed Caption data and for V. Chip Data. If Input **2** is selected and it is 480i (NTSC), then the Microprocessor outputs a Main CCD Select signal from pin **73** to **I005** pin **11** to select 480i input at pin **13**.
- *NOTE: Component inputs other than 480i (NTSC) are not able to display Closed Caption Data.*

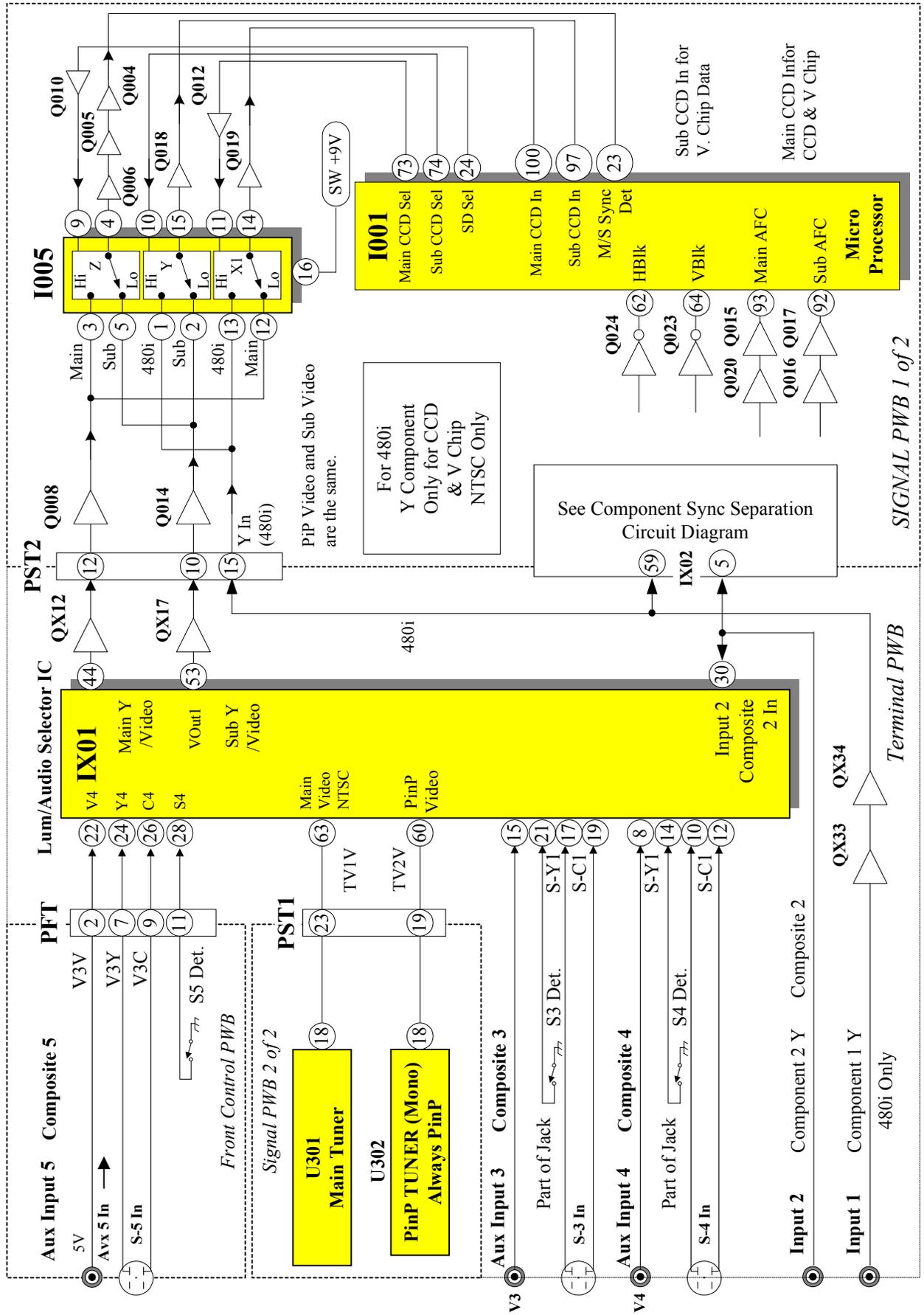
### **(97) Sub CCD IN:**

- The Microprocessor receives Sub Sync information and strips the V Chip Data. This composite sync signal is supplied to the Microprocessor from **I005** pin **15**.
- When an NTSC component input is supplied to Input **2**, this is called 480i. This must also be monitored for V. Chip Data. If Input **2** is selected as PinP source and it is 480i (NTSC), then the Microprocessor outputs a Sub CCD Select signal from pin **74** to **I005** pin **10** to select 480i input at pin **1**.

### **(23) M/S Sync Det (Main / Sub Sync Detection):**

- The composite sync signal from either Main or PinP (Sub) is supplied to the Microprocessor from **I005** pin **4**. The Microprocessor uses the Sync signal to activate the AFC loop, and for Auto Programming. When the channels are changed for the PinP Tuner, the Microprocessor outputs a short control signal from pin **24** (SD Sel) to **I005** pin **9**. **I005** then outputs the Sub composite sync signal input on pin **5**. Normally this IC outputs the Main composite sync signal input on pin **3**.

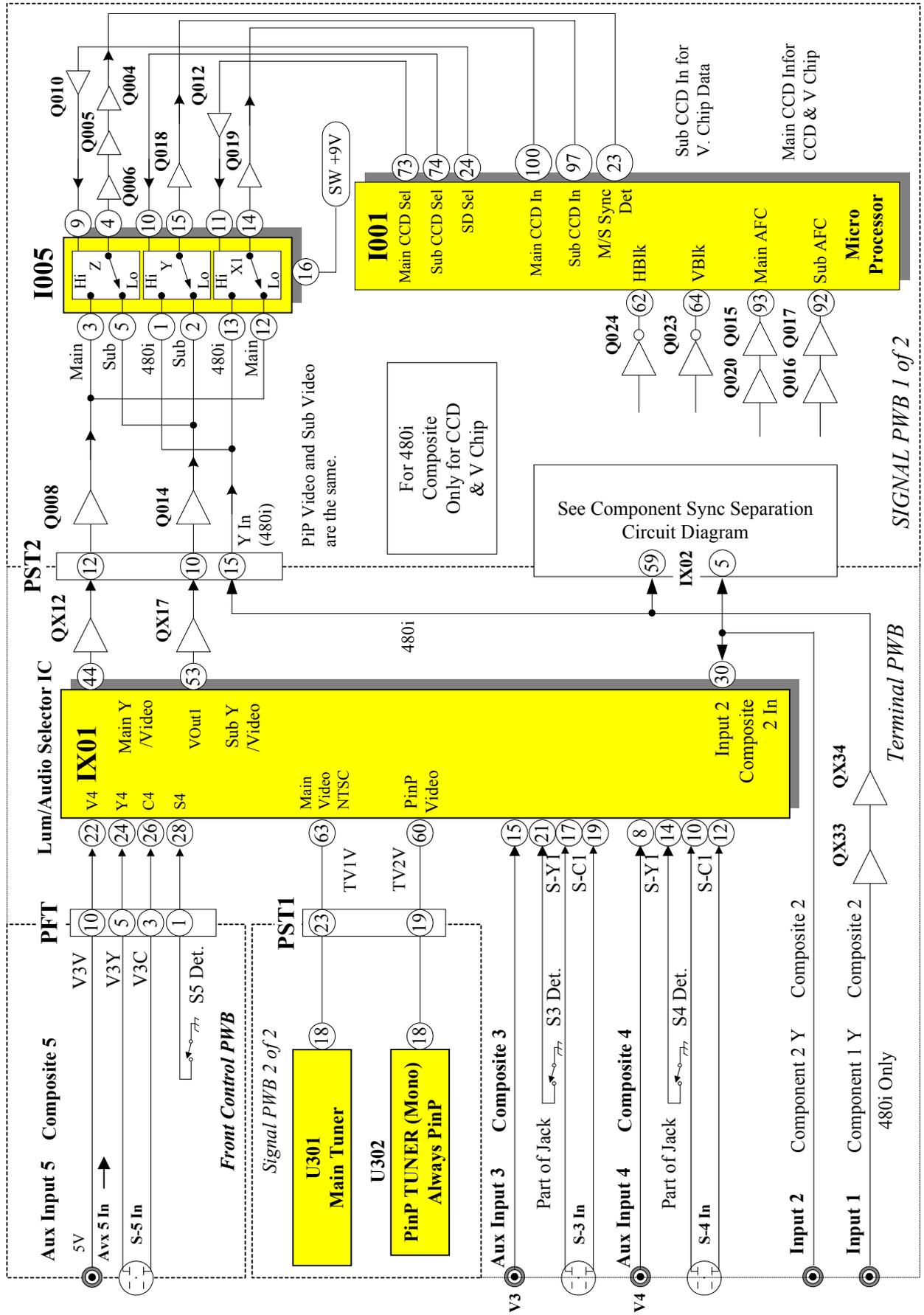
# DP-23, 23G, 27 and DP-27D SERIES CHASSIS NTSC SYNC to MICROPROCESSOR SIGNAL PATH



SIGNAL PWB 1 of 2

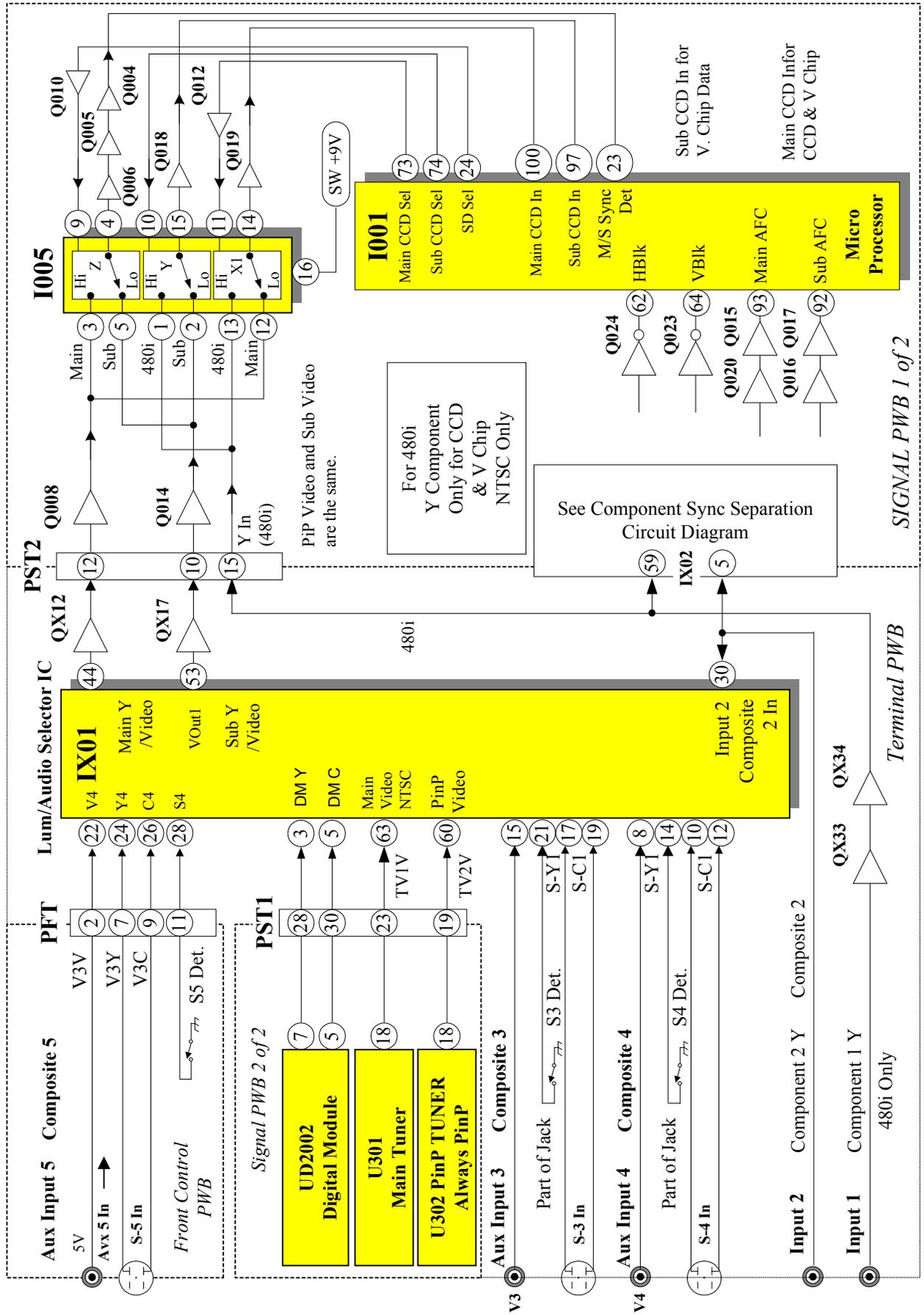
Terminal PWB

# DP-24 Chassis Microprocessor Sync Input



Aux Inputs

# DP-26 SERIES CHASSIS NTSC SYNC to MICROPROCESSOR SIGNAL PATH



Aux Inputs

# **VIDEO INFORMATION**

**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 3**

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## DP-2X NTSC VIDEO SIGNAL PATH CIRCUIT EXPLANATION

*(See DP-2X Chassis Video Signal Path-NTSC Circuit Diagram for details)*

It's important to note that this Chassis horizontal deflection operates at 33.75Khz at all times. Even though this is twice as fast as NTSC, the set will still display NTSC video with no problem. This is accomplished by the Flex Converter. The Flex Converter will manipulate any input, be it NTSC, Component 480i, 480P, 720P, 1080i to the appropriate Horizontal Frequency rate of 33.75Khz. This makes this chassis very versatile in it's application.

The following will discuss the signal flow as show in the above listed Circuit Diagram.

### TUNER INPUTS:

These sets utilizes two tuners, (**DP-26** also has an ATSC Digital Tuner **UD2002**) one for the Main picture **U301** and one for the PinP (Sub) picture **U302**. **U301** is an intergraded tuner with RF front end, IF decoding, Audio Decoding to Lt/Rt. The tuner communicates with the Microprocessor via I2C bus. (See Microprocessor Data Communications Circuit Diagram for details).

The PinP tuner **U302** is also an intergraded tuner, however the Audio output is not used.

Both tuners output their respected composite video via pin 18.

- **U301** Main Tuner Output pin **18** to **PST1** connector pin **23**, to the Selector IC **IX01** pin **63**.
- **U302** PinP (Sub) Tuner Output pin **18** to **PST1** connector pin **19**, to the Selector IC **IX01** pin **60**.

### (DP-26 ONLY):

- **UD2002**
  - ◇ LUMINANCE: The ATSC (QAM) Tuner (Digital Tuner) Outputs DM Y from pin 7 to the PST1 connector pin 28, to the Selector IC IX01 pin 3.
  - ◇ CHROMINANCE: The ATSC (QAM) Tuner (Digital Tuner) Outputs DM C from pin 5 to the PST1 connector pin 30, to the Selector IC IX01 pin 5.

These inputs are used while viewing an SDTV or HDTV source, so that there will be an output from the Monitor Video Jack.

**NOTE:** The DP-26 has a Digital Tuner (ATSC-8VSB and Cable QAM Tuner). This tuner is UD2002 which also is the input/output access for IEEE1394. (See the ATSC Block Diagram which is coming up after the Component, OSD and NTSC Diagram). Even though this explanation is related to NTSC, the ATSC tuner is involved because of the Video Output on the (Monitor Out) jack. When ATSC or QAM is viewed, the monitor out just have video output. This is accomplished by the ATSC (Digital Tuner) having a Y/C output sent to the NTSC circuit for this purpose.

### AUXILIARY INPUT:

This chassis utilizes 5 separate inputs plus a newly added input called **DVI**. The following will break down those input routes to the Selector IC **IX01**.

- (1) **INPUT 1:** This input is only for Component Inputs Y Pr/Pb (31.5Khz to 33.75Khz ATSC) and will not accept Composite on the Y input. Input one's Y line is input directly into **IX02** pin **59** (Y Pr/Pb Selector).
- (2) **INPUT 2:** This input will accept Component Inputs Y Pr/ Pv (31.5Khz to 33.75Khz ATSC) or Y Cr/Cb (15,735Hz. NTSC). It will also accept Composite Video input as long as there is no Pr plug inserted. Input 2 is routed into the Selector IC **IX01** pin **30**.
- (3) **INPUT 3:** This is NTSC composite input only. It also has an accompanying S-Input. Remember that the S-Input takes priority over composite input, when S-Input is active. Input 3 is routed into the Selector IC **IX01** pin **15**. The S-Input inputs are pin **10** for Y (Luminance) and pin **17** for C (Chroma). When an S-Jack is inserted into the plug, an internal mechanical switch is activated which produces a low to the Selector IC **IX01** pin **21** and the Selector IC notifies the Microprocessor that and S-Jack is installed.
- (4) **INPUT 4:** This is NTSC composite input only. It also has an accompanying S-Input. Remember that the S-Input takes priority over composite input, when S-Input is active. Input 4 is routed into the Selector IC **IX01** pin **8**. The S-Input inputs are pin **8** for Y (Luminance) and pin **12** for C (Chroma). When an S-Jack is inserted into the plug, an internal mechanical switch is activated which produces a low to the Selector IC **IX01** pin **14** and the Selector IC notifies the Microprocessor that and S-Jack is installed.
- (5) **INPUT 5:** On the Front Control Panel. This is NTSC composite input only. It also has an accompanying S-Input. Remember that the S-Input takes priority over composite input, when S-Input is active. Video Input 5 is routed through the **PFT** connector pin **2** (pin **10** for DP24 only), into the Selector IC **IX01** pin **22**. The S-Input inputs are routed through the **PFT** connector pin **7** (pin **5** for DP24 only) for Y and pin **9** (pin **3** for DP24 only) for C, into the Selector IC **IX01** pin **24** for Y (Luminance) and pin **26** for C (Chroma). When an S-Jack is inserted into the plug, an internal mechanical switch is activated which produces a low through the **PFT** connector pin **11** (pin **1** for DP24 only), into the Selector IC **IX01** pin **28** and the Selector IC notifies the Microprocessor that and S-Jack is installed.

*(Continued on page 03-02)*

## DP-2X NTSC VIDEO SIGNAL PATH CIRCUIT EXPLANATION

*(Continued from page 03-01)*

### COMPOSITE VIDEO PATH:

When a composite input is selected, it must be broken down into its respective parts, Y and C. This is accomplished for the Main video by the 3D Y/C and for the PinP (Sub) picture by the 2-Line Comb filter.

**MAIN:** The Main composite output is routed out of the Selector IC **IX01** pin **44** to **QX13**. Then through the video low pass filter comprised of **QW01**, **QW02**, and **QW04**. It arrives at the 3D Y/C chip **IW01** pin **88**. Here the composite video is separated into Y/C 3D enhanced, and output on the following pins, Y from pin **84** and C from pin **83**.

### Y COMPONENT (For Composite In).

The Y component is then routed through a low pass filter comprised of **QW09**, LPF **XW01**, **QW10**, and **QW12** into the Main Video/Chroma Processor IC **IZ02**.

Note too that the Y component is also routed into the PinP (Sub) Video/Chroma Processor IC **IZ01** pin **2**. This is for when the customer presses the Swap button when the PinP Sub window is on.

### C COMPONENT: (For Composite In).

The C component is then routed through a low pass filter comprised of **QW13**, LPF **XW02**, **QW14**, and **QW15**. Then the chroma must be routed through the TILT circuit. This circuit compensates for the phase relationship of flesh tones between composite and component. This circuit is comprised of **QZ04** and **QZ05**. Not shown is the switch that enables this phase rotation circuit. The output control is from the selector IC **IX01** pin **59** to **QZ07**. From **QZ05** the Chroma component is routed into pin **16** of the Main Video/Chroma Processor IC **IZ02**.

Note too that the Chroma component is also routed into the PinP (Sub) Video/Chroma Processor IC **IZ01** pin **16**. This is for when the customer presses the Swap button when the PinP Sub window is on.

### S-INPUT 3, 4 and/or 5:

When the S-Input is selected, it already is separated into its Y and C components. In this case, it is routed directly into the Main Video Chroma Processor **IZ02**. It is output from the Selector IC **IX01** pin **44**, through **QX13**, **QX25**, and into the Main Video Chroma Processor **IZ02** pin **4**. The Chroma component is output from the Selector IC **IX01** pin **47**, through **QX14**, **QX26**, and into the Main Video Chroma Processor **IZ02** pin **19**.

The responsibility of **IZ02** is to now convert the separated Y/C components of the Main picture into a usable format for the Flex Converter. The Flex Converter **FC4** utilizes component inputs Y Pr/Pb or Y Cr/Cb. **IZ02** outputs only NTSC, so its output are Y Cr/Cb. Y from pin **24**, Cr from pin **22**, and Cb from pin **23**.

Y is then routed through **QZ10** to the connector **PST1** pin **7**.

Cr is then routed through **QZ08** to the connector **PST1** pin **4**.

Cb is then routed through **QZ09** to the connector **PST1** pin **5**.

*(See the DP-2X Chassis Video Signal Path-NTSC, Component, OSD for continuation).*

### PinP (Sub) Video Path:

The PinP (Sub) composite video is output from the Selector IC **IX01** pin **53**, through **QV09**, **QV10**, and into the 2-Line Comb Filter **IV01** pin **4**. It is separated into its individual Y/C components.

The Y (Luminance) component of the PinP (Sub) picture is then output pin **15**, through **QV01**, low pass filter **XV01**, through **QV02**, **QV04** and back into the Selector IC **IX01** pin **49**.

The C (Chroma) component of the PinP (Sub) picture is then output pin **13**, through **QV05**, low pass filter **XV02**, through **QV06**, **QV08** and back into the Selector IC **IX01** pin **51**.

From here, the Selector IC **IX01** output the Y from pin **56** through **QX15**, **QX27** into the PinP (Sub) Video/Chroma Processor **IZ01** pin **4**.

The C component from pin **58** through **QX16**, **QX28** into the PinP (Sub) Video/Chroma Processor **IZ01** pin **19**.

**IZ01:**

The responsibility of **IZ01** is to now convert the separated Y/C components of the PinP (Sub) picture into a usable format for the Flex Converter. The Flex Converter **FC4** utilizes component inputs Y Pr/Pb or Y Cr/Cb. **IZ01** outputs only NTSC, so its output are Y Cr/Cb. Y from pin **24**, Cr from pin **22**, and Cb from pin **23**.

Y is then routed through **QZ01** to the connector **PST2** pin **23**.

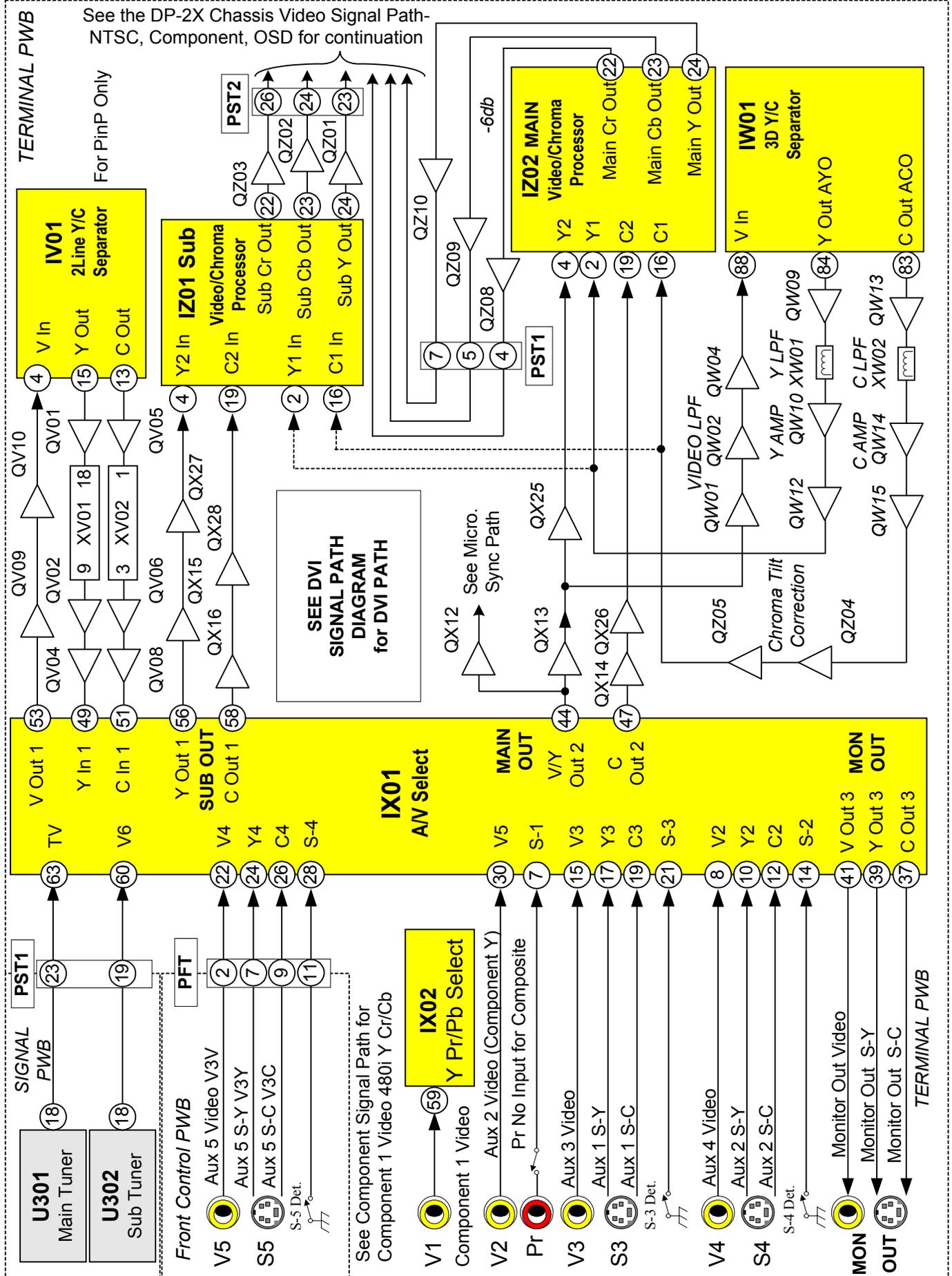
Cr is then routed through **QZ03** to the connector **PST2** pin **26**.

Cb is then routed through **QZ02** to the connector **PST2** pin **24**.

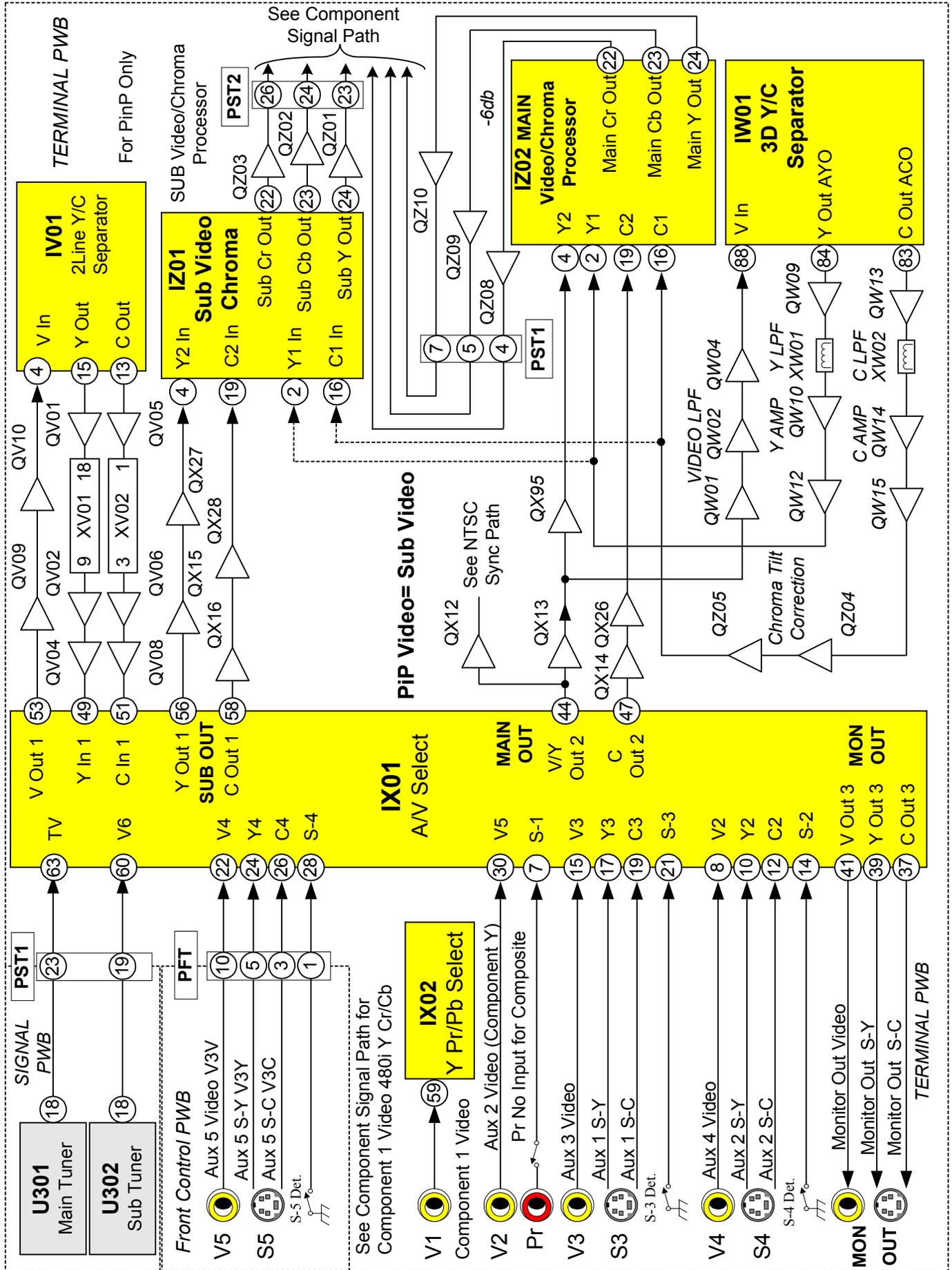
*(See the DP-2X Chassis Video Signal Path-NTSC, Component, OSD for continuation).*

**NOTE:** The DP-23, 23G, 26, 27 and 27D all have a DVI input. Shown in the Component input path.  
The DP-24 Does NOT have a DVI input.

# DP-23, DP-23G, DP-27 and DP-27D CHASSIS VIDEO SIGNAL PATH - NTSC



# DP-24 Chassis Video NTSC

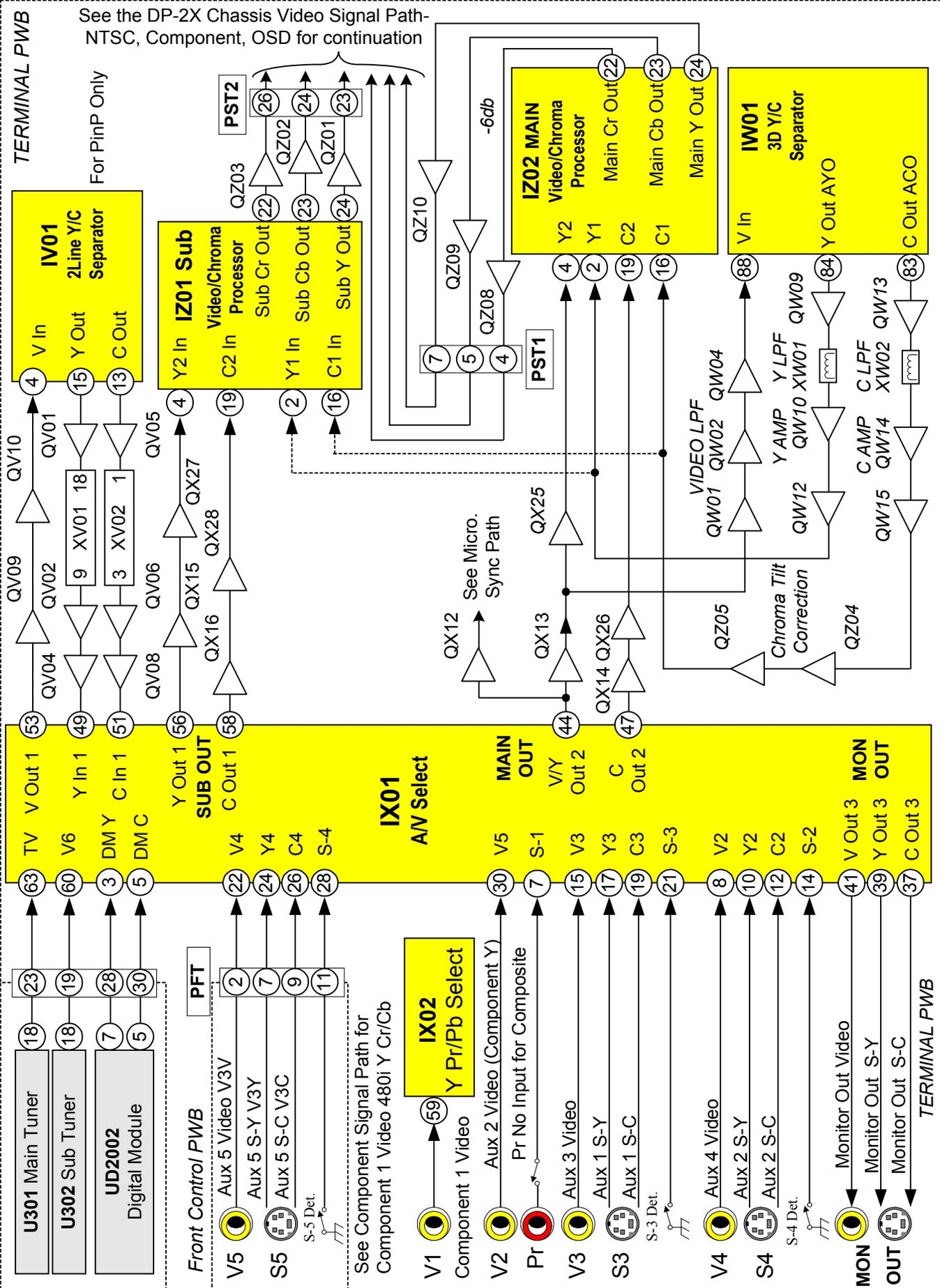


# DP-26 CHASSIS VIDEO SIGNAL PATH - NTSC

SEE DVI SIGNAL PATH DIAGRAM for DVI PATH

SIGNAL PWB

PST1



TERMINAL PWB

See the DP-2X Chassis Video Signal Path-NTSC, Component, OSD for continuation

For PinP Only

See Component Signal Path for Component 1 Video 480i Y Cr/Cb

## DP-2X CHASSIS VIDEO SIGNAL PATH-NTSC, COMPONENT, OSD CIRCUIT EXPLANATION

*(See the Chassis Video Signal Path-NTSC, Component, OSD for details)*

*(See Video Signal Path-NTSC Circuit Diagram for details about NTSC)*

It's important to note that this Chassis horizontal deflection operates at 33.75Khz at all times. Even though this is twice as fast as NTSC, the set will still display NTSC video with no problem. This is accomplished by the Flex Converter. The Flex Converter will manipulate any input, be it NTSC, Component 480i, 480P, 720P, 1080i to the appropriate Horizontal Frequency rate of 33.75Khz. This makes this chassis very versatile in it's application.

The following will discuss the Component signal path and the continuation of the NTSC signal path.

### COMPONENT INPUTS 1 and/or 2:

This chassis utilizes 5 separate inputs plus a newly added input called **DVI**. The following will break down those input routes to the Y Pr/Pb Selector IC **IX02**.

- (1) **INPUT 1:** This input is only for Component Inputs Y Pr/Pb (31.5Khz to 33.75Khz ATSC) and will not accept Composite on the Y input.
  - The Y line is input directly into the Y Pr/Pb Selector **IX02** pin **59**.
  - The Cr/Pr line is input directly into the Y Pr/Pb Selector **IX02** pin **63**.
  - The Cv/Pb line is input directly into the Y Pr/Pb Selector **IX02** pin **62**.
- (2) **INPUT 2:** This input will accept Component Inputs Y Pr/ Pv (31.5Khz to 33.75Khz ATSC) or Y Cr/Cb (15,735Hz. NTSC). It will also accept Composite Video input as long as there is no Pr plug inserted.
  - The Y line is input directly into the Y Pr/Pb Selector **IX02** pin **5**.
  - The Cr/Pr line is input directly into the Y Pr/Pb Selector **IX02** pin **9**.
  - The Cv/Pb line is input directly into the Y Pr/Pb Selector **IX02** pin **7**.
  - Input 2 Composite Video is routed into the Selector IC **IX01** pin **30**.
- (3) **DVI INPUT** (Digital Video Interface): This input will accept Component Inputs Y Pr/ Pv (31.5Khz to 33.75Khz ATSC) only. *(See DVI Signal Path for further details). (NOT in the DP24 Chassis).*
  - The Y line is input from the **PET** connector pin **5** into the Y Pr/Pb Selector **IX02** pin **53**.
  - The Pr line is input from the **PET** connector pin **3** into the Y Pr/Pb Selector **IX02** pin **57**.
  - The Pb line is input from the **PET** connector pin **7** into the Y Pr/Pb Selector **IX02** pin **55**.
- (4) **DIGITAL TUNER (ATSC) UD2002 INPUT:** These inputs are provided from the Digital Tuner (ATSC). The ATSC Tuner output DM-Y, DM-Pb and DM-Pr. (Only in the DP26 Chassis). *(See DP-26 Component, OSD, NTSC Signal Path for specifics).*
  - DM-HY (Luminance) from **PMS2** pin **16**, through **PST1** pin **13** to Y Pr/Pb Selector **IX02** pin **15**.
  - DM-Pb (Blue Chroma) from **PMS2** pin **14**, through **PST1** pin **15** to Y Pr/Pb Selector **IX02** pin **17**.
  - DM-Pr (Red Chroma) from **PMS2** pin **12**, through **PST1** pin **17** to Y Pr/Pb Selector **IX02** pin **19**.
  - ♦ **NOTE:** When receiving a SDTV or HDTV signal, the Digital Module also outputs Composite Video/ Chroma for the Monitor Output. *(See DP-26 NTSC Signal Path for specifics).*

### COMPONENT VIDEO PATH:

The output from the Y Pr/Pb Selector **IX02** is then routed to the Video/Chroma Y Pr/Pb Switch.

**IZ01** is used to select the PinP (Sub) picture source. Either from component inputs or from the separated NTSC inputs as described in the DP-2X Chassis Video Signal Path-NTSC Circuit Diagram.

- The Sub Y component is output from the pin **50** through **QX19** into the PinP (Sub) Video/Chroma Y Pr/Pb Switch **IZ01** pin **30**.
- The Sub Cr/Pr component is output from the pin **46** through **QX21** into the PinP (Sub) Video/Chroma Y Pr/Pb Switch **IZ01** pin **28**.
- The Sub Cb/Pb component is output from the pin **48** through **QX20** into the PinP (Sub) Video/Chroma Y Pr/Pb Switch **IZ01** pin **29**.
- Main NTSC Y component is input into the PinP (Sub) Video/Chroma Y Pr/Pb Switch **IZ01** pin **2**.
- PinP (Sub) NTSC Y component is input into the PinP (Sub) Video/Chroma Y Pr/Pb Switch **IZ01** pin **4**.

**IZ02** is used to select the Main picture source. Either from component inputs or from the separated NTSC inputs as described in the DP-2X Chassis Video Signal Path-NTSC Circuit Diagram.

- The Main Y component is output from the pin **44** through **QX24** into the Main Video/Chroma Y Pr/Pb

*(Continued on page 7)*

## DP-2X CHASSIS VIDEO SIGNAL PATH-NTSC, COMPONENT, OSD CIRCUIT EXPLANATION

Switch **IZ02** pin **30**.

- The Main Cr/Pr component is output from the pin **40** through **QX22** into the Main Video/Chroma Y Pr/Pb Switch **IZ02** pin **28**.
- The Main Cb/Pb component is output from the pin **42** through **QX23** into the Main Video/Chroma Y Pr/Pb Switch **IZ02** pin **29**.
- Main NTSC Y component is input into the Main Video/Chroma Y Pr/Pb Switch **IZ02** pin **2**.
- PinP (Sub) NTSC Y component is input into the Main Video/Chroma Y Pr/Pb Switch **IZ02** pin **4**.

### To the Flex Converter U303:

After the selection has been made as to the source for the Main and PinP (Sub) picture, **IZ01** and **IZ02** output the appropriate signal. **IZ01** outputs the PinP (Sub) picture and **IZ02** outputs the Main picture.

(1) **OUTPUT from IZ02 Main Picture:** This output is routed from;

- Main Y component Pin **24** through **QZ10** to the connector **PST1** pin **7**. Here the signal is split.
  - ◊ The primary path is through **Q306** to the Flex Converter U303 connector **PFC1** pin **3**.
  - ◊ The secondary path is for 1080i input signals ONLY. In this case, the signal is input directly into the Rainforest IC. The path is through **Q406** and into the Rainforest IC **I401** pin **8**.
- Main Cr/Pr component Pin **22** through **QZ08** to the connector **PST1** pin **4**. Here the signal is split.
  - ◊ The primary path is through **Q308** to the Flex Converter U303 connector **PFC1** pin **5**.
  - ◊ The secondary path is for 1080i input signals ONLY. In this case, the signal is input directly into the Rainforest IC. The path is through **Q405** and into the Rainforest IC **I401** pin **9**.
- Main Cb/Pb component Pin **23** through **QZ09** to the connector **PST1** pin **5**. Here the signal is split.
  - ◊ The primary path is through **Q307** to the Flex Converter U303 connector **PFC1** pin **4**.
  - ◊ The secondary path is for 1080i input signals ONLY. In this case, the signal is input directly into the Rainforest IC. The path is through **Q405** and into the Rainforest IC **I401** pin **9**.

(2) **OUTPUT from IZ01 PinP (Sub) Picture:** This output is routed from;

- PinP (Sub) Y component Pin **24** through **QZ01** to the connector **PST2** pin **23**. Then to the Flex Converter U303 connector **PFC1** pin **17**.
- PinP (Sub) Cr/Pr component Pin **22** through **QZ03** to the connector **PST2** pin **26**. Then to the Flex Converter U303 connector **PFC1** pin **19**.
- PinP (Sub) Cb/Pb component Pin **23** through **QZ02** to the connector **PST2** pin **24**. Then to the Flex Converter U303 connector **PFC1** pin **18**.

### FLEX CONVERTER OUTPUT:

The Flex Converter outputs only one horizontal frequency and that is 33.75Khz (540P) which relates specifically to 1080i deflection rate. So in other words, all inputs are upconverted to the higher deflection rate. 1080i is routed directly to the Rainforest IC **I401** and has no need for Flex Converter manipulation.

**This can be a trouble shooting tool if the Flex Converter is suspected as having problems.** Simply input a true 1080i signal and bypass the Flex Converter.

The output from the Flex Converter is as follows;

- Y is output from pin **16** of the **PFC2** connector, through **Q403** and into the Rainforest IC pin **3**.
- Pr is output from pin **20** of the **PFC2** connector, through **Q401** and into the Rainforest IC pin **5**.
- Pb is output from pin **18** of the **PFC2** connector, through **Q402** and into the Rainforest IC pin **4**.

### RAINFOREST IC I401:

This IC processes the input signal source, adjust brightness, contrast, color, tint, etc... and add (if necessary) PinP (Sub) picture information and/or OSD information and output the Main Picture as R, G and B.

Red is output pin **43**, Blue is output pin **41** and Green is output pin **42**.

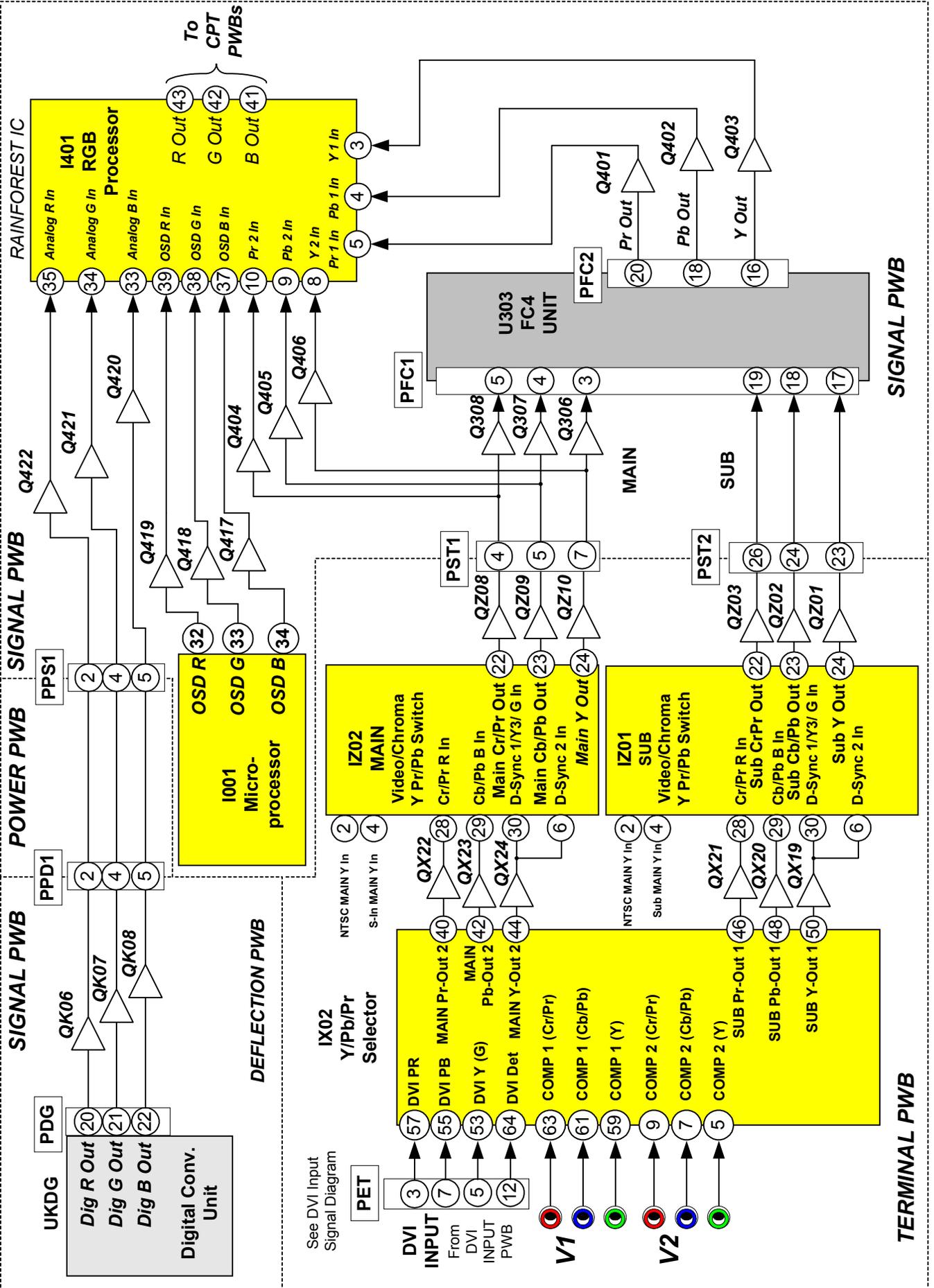
### OSD:

OSD can be introduced via the Microprocessor and/or in the same fashion the Digital Convergence Module can introduce it's information. OSD from Microprocessor is Red pin **39**, Blue pin **37** and Green pin **38**.

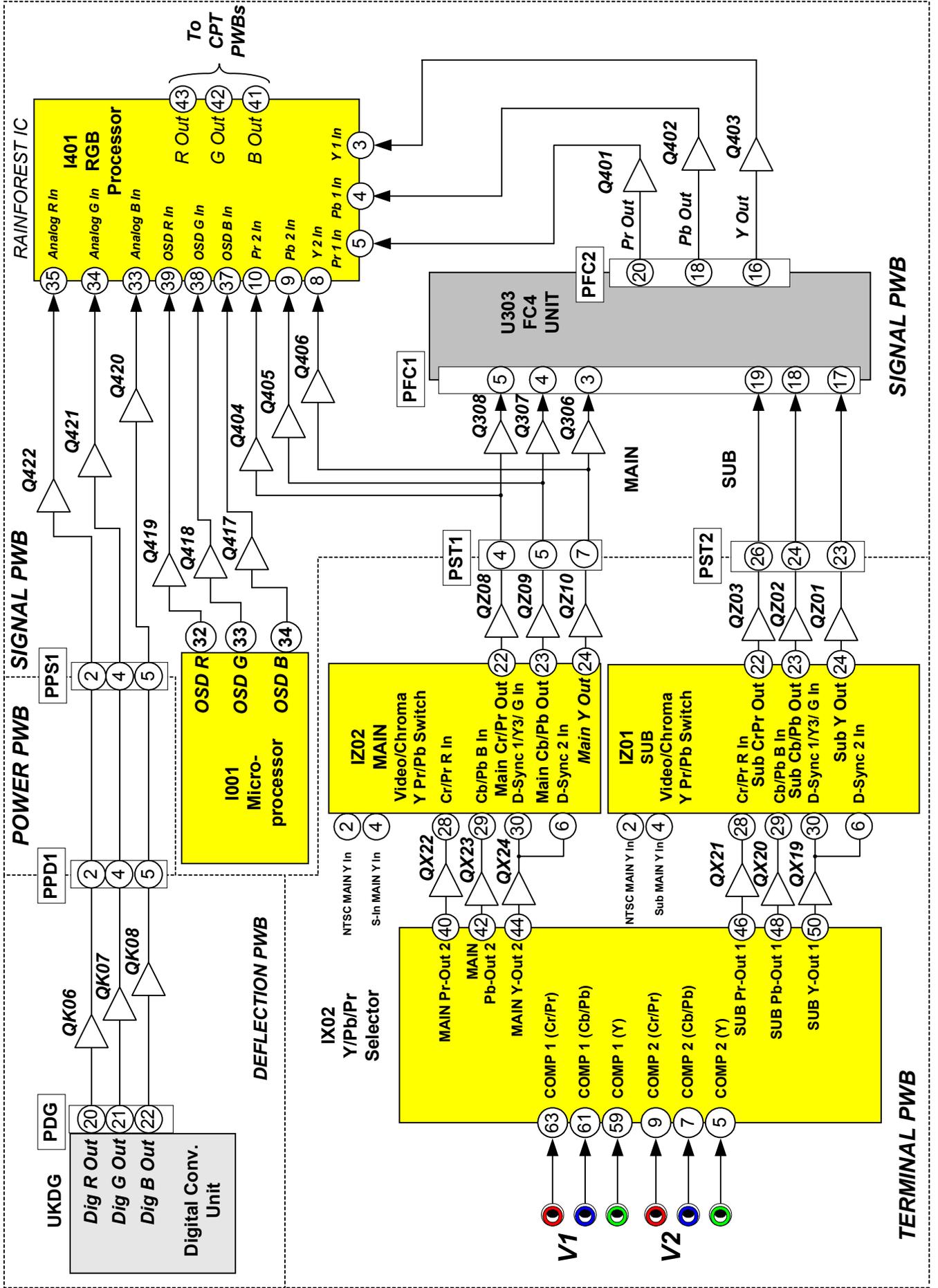
Digital Convergence Information is input Red pin **35**, Blue pin **33** and Green pin **34**.

(See *Digital Convergence Interface Circuit Diagram Explanation for details*).

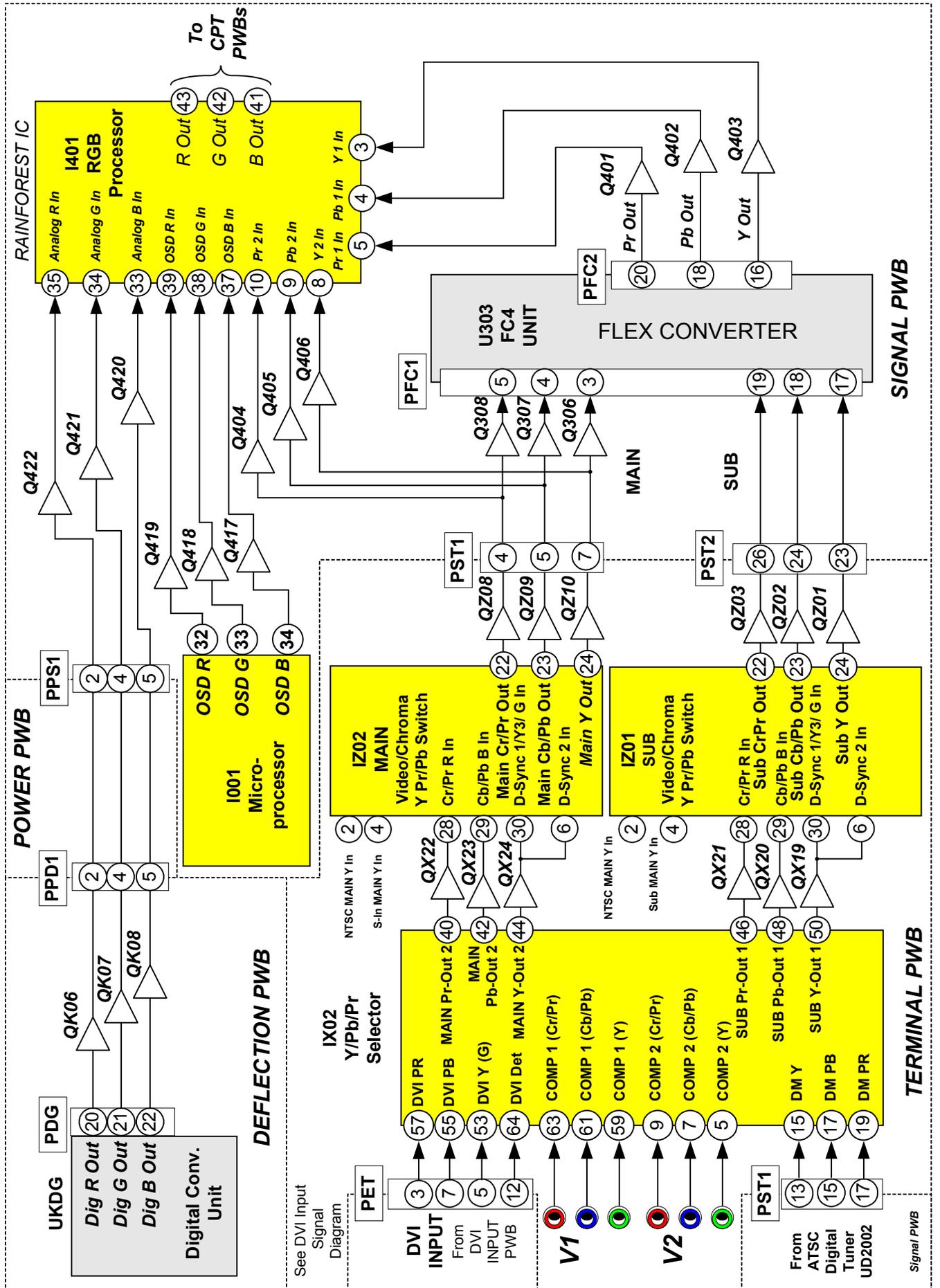
# DP-23, DP-23G, DP-27 and DP-27D Chassis Video Signal Path - NTSC, Component, OSD



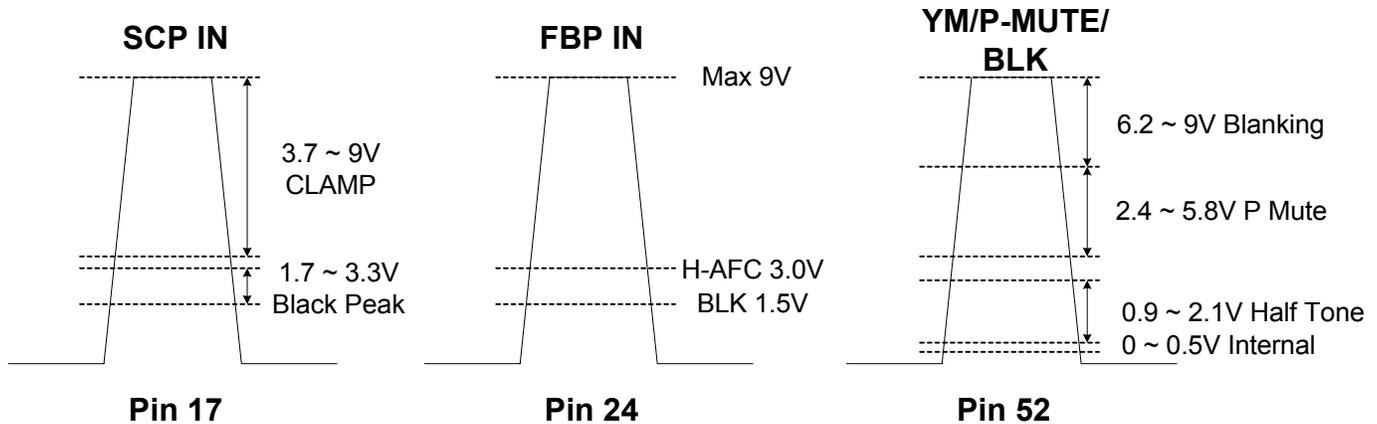
# DP-24 Chassis Video Component OSD & NTSC



# DP-26 Chassis Video Signal Path - NTSC, Component, OSD



## DP-2X RAINFOREST IC INFORMATION (I401)



### Pin 17 = SCP.

**Black Peak:** This input is utilized for establishing the Black Peak level used in Black Peak expansion circuit. Here the Black Peak is expanded towards Black to increase the contrast ratio.

**CLAMP:** The clamp pulse is utilized for DC restoration and blanking timing.

### Pin 24 = FBP. Combination of the following.

**Fly back pulse: 1.5V ~ 3.0V H-AFC:** This input is received from the Horizontal Blanking (H. Blk) signal generated in the Deflection circuit by Q706. This signal is used as a sample pulse in the Horizontal AFC circuit, which synchronizes the Horizontal Drive signal with the incoming Video sync signal input at pin 16. In Through Mode, pin 8.

**Fly back pulse: 3.0V ~ 9.0V Max:** This input is received from the Flex Converter and is a combination of Horizontal and Vertical blanking signals.

H Blk from the Flex Converter Pin 12 through Q412

V Blk from the Flex Converter Pin 11 through Q411

Used within the Rainforest is for DC restoration, Pedestal level detection and Clamping signals, such as Burst Gate Pulse.

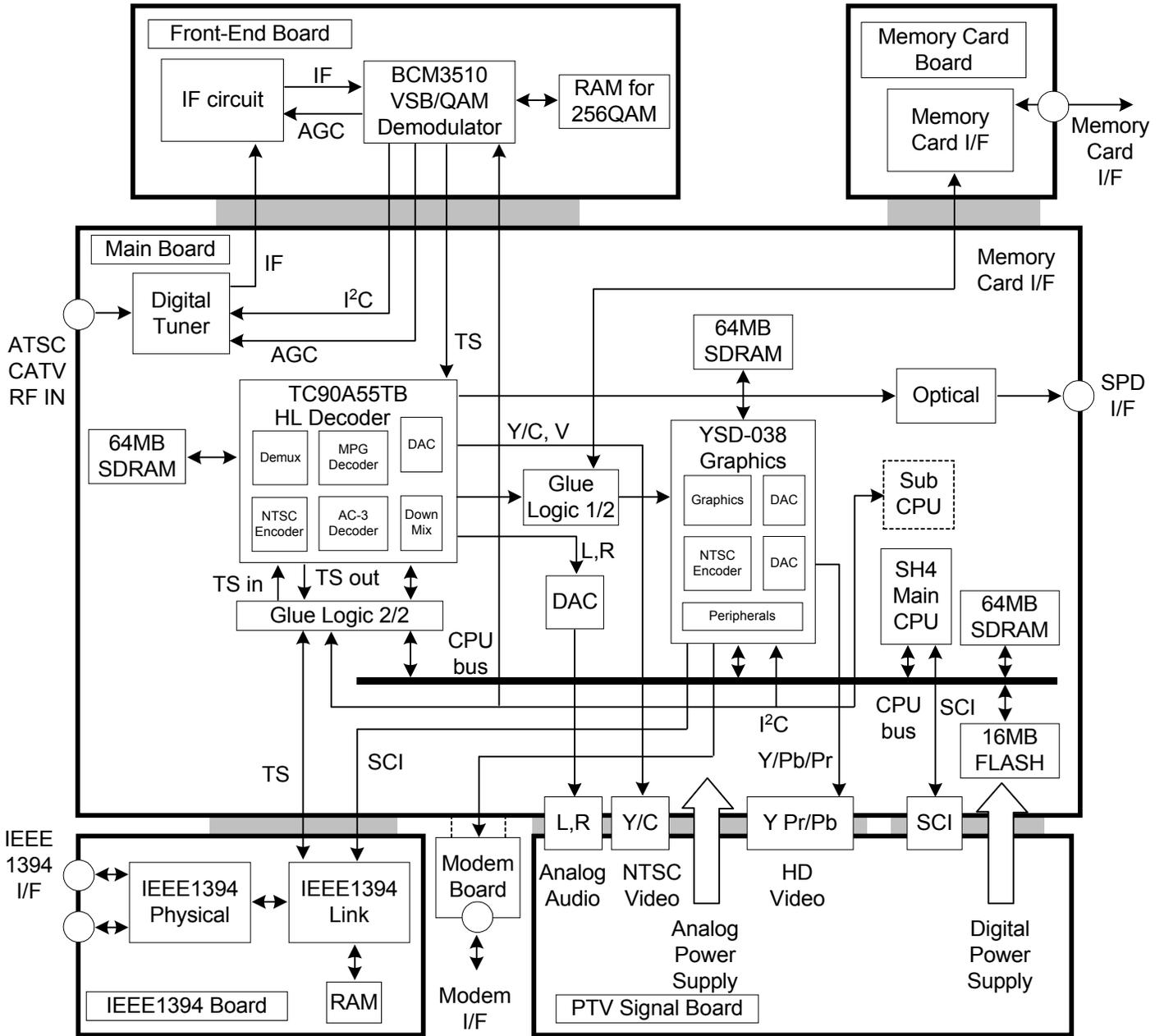
### Pin 52 = YM/P-MUTE/BLK. Combination of the following.

**INTERNAL:** 0.0V ~ 0.5V Used internal within the Rainforest IC.

**HALFTONE:** 0.9V ~ 2.1V: This input is received from the Microprocessor and is used to establish the Transparency effect of OSD. This also mutes the video in exact timing with On Screen Display pulses (OSD). Half Tone from the Microprocessor Pin 22 through Q415.

**P MUTE:** 2.4V ~ 5.8V: Not Used.

## Block Diagram of UD2002 ATSC / QAM / IEEE1394 Interface Module



## DP-2X ABL CIRCUIT EXPLANATION

(See ABL Circuit Diagram for details)

The ABL voltage is generated from the ABL pin (3) of the Flyback transformer **TH01**. The ABL pull-up resistors are **RH27** and **RH28**. They receive their pull up voltage from the **SW +115V B+** line for Deflection generated from the Power Supply.

### ABL VOLTAGE OPERATION

The ABL voltage is determined by the current draw through the Flyback transformer. As the picture brightness becomes brighter or increases, the demand for replacement of the High Voltage being consumed is greater. In this case, the Flyback will work harder and the current through the Flyback increases. This in turn will decrease the ABL voltage. The ABL voltage is inversely proportionate to screen brightness.

Also connected to the ABL voltage line is **DH16**. This zener diode acts as a clamp for the ABL voltage. If the ABL voltage tries to increase above 9V due to a dark scene which decreases the current demand on the flyback, the ABL voltage will rise to the point that **DH16** dumps the excess voltage into the 9V line.

### ACCL TRANSISTOR OPERATION

The ABL voltage is routed through the **PPD2** connector pin 3 to the Power Supply PWB, then to **PPS2** connector pin 3 to the Signal PWB. Then the ABL voltage is routed through the acceleration circuit **RA54** and **D404** to the base of **Q413**. Under normal conditions, this transistor is nearly saturated. **Q413** determines the voltage being supplied to the cathode of **D403**, which is connected to pin 53 of the Rainforest IC, **I401**. During an ABL voltage decrease due to an excessive bright circumstance, the base of **Q413** will go down, this will drop the emitter voltage which in turn drops the cathode voltage of **D403**. This in turn will pull voltage away from pin 53 of the Rainforest IC, **I401**. Internally, this reduces the contrast and brightness voltage which is being controlled by the I<sup>2</sup>C bus data communication from the Microprocessor arriving at pins 30 and 31 of the Rainforest IC and reduces the overall brightness, preventing blooming as well as reducing the Color saturation level to prevent color smear.

### ABL SWITCH QH03

New for this chassis is the ability to change the brightness level of the Side Panels when watching a NTSC 4X3 image. When a 4X3 images is displayed on a 16X9 set, the sides do not reach the edges. To avoid excessive ageing at the 4X3 display area, the side panels IRE levels are raised. However, sometimes the customer may want to turn the side gray panels off. Through the Video Advanced features Menu the customer can now do this. When the Side panels are turned off, the overall average ABL level for the image is reduced. To compensate, **QH03** ABL Switch is added. When the customer selects Black Side panels, the Microprocessor **I001** tells the Rainforest IC **I401** via I<sup>2</sup>C communication to output a high from the DAC2 line pin 36. This high is routed through the **PPS2** connector pin 2 on the Signal PWB to the Power Supply PWB. Then from the **PPD2** connector pin 2 on the Power Supply PWB to the **PPD2** connector on the Deflection PWB and finally to the base of **QH03** turning it **On**.

With **QH03** turned on, the Resistor **RH29** connected to the collector is added to the ABL pull up circuit and the ABL level drops slightly to compensate for the side panel loss of brightness.

The Difference between chassis for the ABL circuit relate to the values of Resistors **RH24**, **RH25** and **RH32**. See diagram for details.

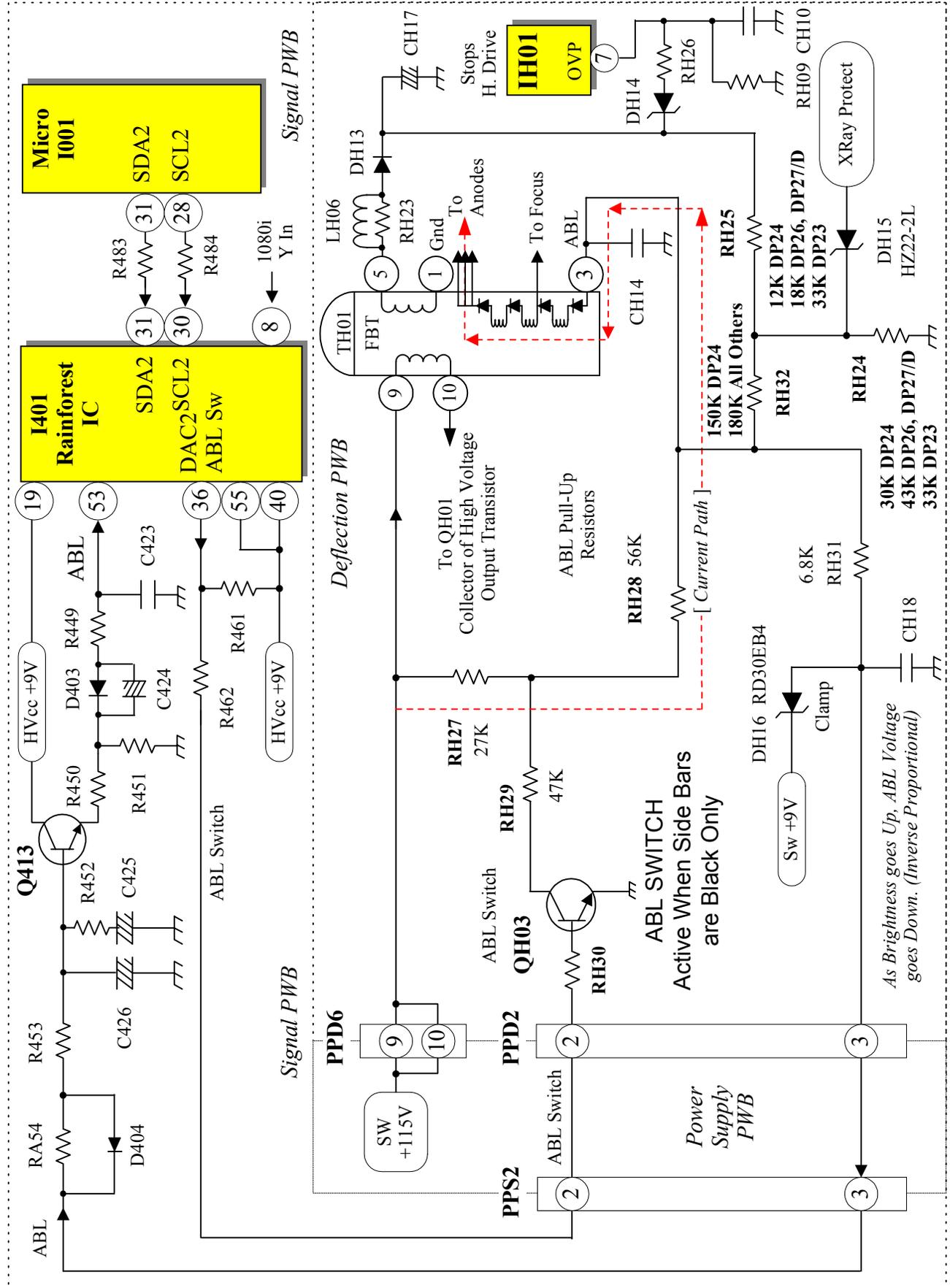


Gray Side Bars

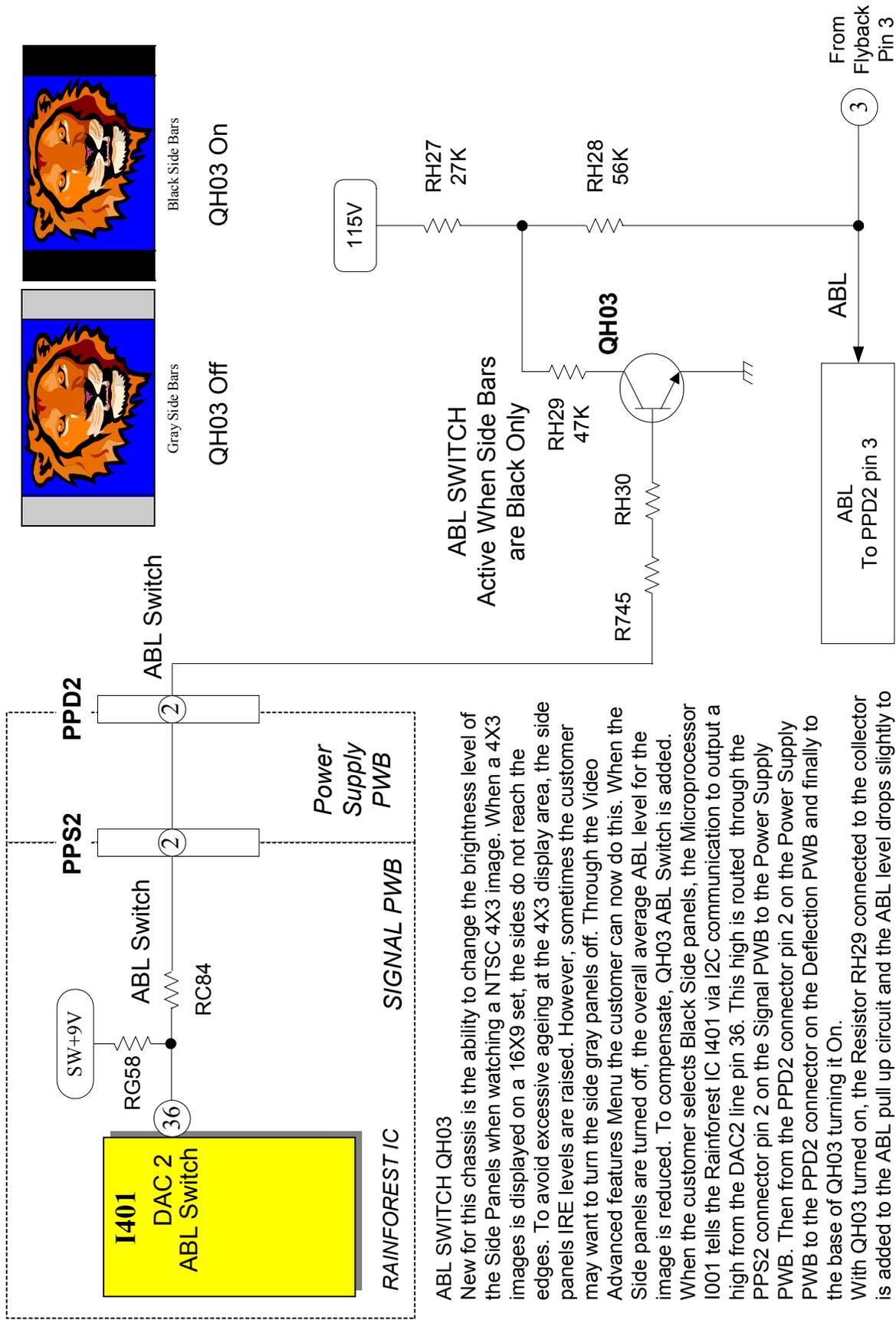


Black Side Bars

# DP-2X Chassis A.B.L. Circuit Diagram



# DP-2X ABL SWITCH FOR 4X3 DISPLAY WITH BLACK SIDE BARS MODE ONLY



ABL SWITCH QH03  
 New for this chassis is the ability to change the brightness level of the Side Panels when watching a NTSC 4X3 image. When a 4X3 image is displayed on a 16X9 set, the sides do not reach the edges. To avoid excessive ageing at the 4X3 display area, the side panels IRE levels are raised. However, sometimes the customer may want to turn the side gray panels off. Through the Video Advanced features Menu the customer can now do this. When the Side panels are turned off, the overall average ABL level for the image is reduced. To compensate, QH03 ABL Switch is added. When the customer selects Black Side panels, the Microprocessor I001 tells the Rainforest IC I401 via I2C communication to output a high from the DAC2 line pin 36. This high is routed through the PPS2 connector pin 2 on the Signal PWB to the Power Supply PWB. Then from the PPD2 connector pin 2 on the Power Supply PWB to the PPD2 connector on the Deflection PWB and finally to the base of QH03 turning it On. With QH03 turned on, the Resistor RH29 connected to the collector is added to the ABL pull up circuit and the ABL level drops slightly to compensate for the side panel loss of brightness.

## DP-2X AUDIO VIDEO MUTE CIRCUIT EXPLANATION

(See DP-2X Series Chassis Audio Video Mute Circuit Diagram for details)

There are times in which the main picture and audio must be muted. This can be because of changing channels where the noise between stations is unacceptable, same thing for Auto Programming channels. When the deflection circuit malfunctions, etc...

All this is done primarily to prevent damage to the CRTs or to external amplifiers or speakers connected to the projection television.

### **MICROPROCESSOR OUTPUT:**

The Microprocessor outputs V. Mute from pin **49** when changing channels, Auto Programming, etc... This high is routed to the Video Mute circuit and to the Audio Mute circuit.

### **VIDEO MUTE PATH.**

The High from pin **49** is routed to **D412** to the base of **Q442**. The following action will be labeled MUTE ACTIVATION for here forward, please use the below explanation when Mute Activation is mentioned.

### **MUTE ACTIVATION:**

When **Q442** turn on, the collector pulls the base of **Q441** low and turns it on. It's collector is connected to the HVcc 9V line through **R551** and **D411**. When **Q441** turns on, it's collector goes high. This is routed to two places. Through **R441**, **D402**, and **R439** and into the Rainforest IC pin **24** of **I401**. This pin is also the same pin that FC H Blk and FC V Blk is input. Generally this input is a positive going pulse that blanks the video during the peak pulses. However, when the DC component is forced high by the action of **Q411** turning on, this pin goes high and mutes the output of RGB.

The other route for the high from **Q411** is through **R548** to the base of **Q440**. This transistor turns On and outputs the high from it's collector out it's emitter to mute the Audio described later.

Another circuit attached to the *Mute Activation* circuit is AC Loss Detection.

### **AC LOSS DETECTION:**

AC is monitored by the AC Loss detection circuit. The AC input from **I903** to **PPS3** pin (1) on the Power Supply PWB is routed and rectified by **D416**. This charges up **C561** and through **D415** to charge **C467**. When AC is first applied, **C467** charges slightly behind **C561** preventing activation of **Q445**. If AC is lost, **C561** discharges rapidly pulling the base of **Q445** low, however **D415** blocks **C467** from discharging and the emitter of **Q445** is held high. This action turns on **Q445** and produces a high on it's collector. This high is routed to the base of **Q442**. See the *Mute Activation* circuit explained previously.

### **SPOT:**

SPOT is generated from the deflection PWB when either Horizontal or Vertical deflection is lost. This is to prevent a horizontal or vertical line from being burnt into the CRTs. See *Horizontal and Vertical Sweep Loss Detection circuit and explanation and circuit diagram for details*. This high is input from **PPD2** pin (4), through **PPS2** pin (4), **D413** to the base of **Q442**. See the *Mute Activation* circuit explained previously.

### **H Blk Loss Det:**

If the Horizontal Blanking signal is loss to the Signal PWB, **Q444** will detect the loss. Normally, **Q444** is supplied with H. Blanking on it's base. By the activity of the pulse charging **C466**, the base of **Q443** and it's emitter are held high. If H. Blk is lost, then **C466** will discharge through **R558**. **C465** is blocked by **D414** and it holds the emitter of **Q443** high. This action turns on **Q443** and supplies a high to the base of **Q442**. See the *Mute Activation* circuit explained previously.

See next page for continuation of Audio Mute Circuit explanation.

## DP-2X AUDIO VIDEO MUTE CIRCUIT EXPLANATION

### **AUDIO MUTE PATH: Labeled as V MUTE 2:**

See the *Mute Activation* circuit explained previously.

When Q441 collector is high, the base of Q440 is high. This turns it on and supplies a high from the emitter. This high is routed to the following circuits;

### **OUT TO HI-FI MUTE PATH: Labeled as V MUTE 2:**

The high from Q440 is routed to DA03 anode. Then DA01, and DA02 fire and supply the high to the bases of QA07 and QA08. These in turn ground out the audio for Out to Hi-Fi audio output jacks.

Also, the high from the Microprocessor pin 71 to I007 (in pin 7 at 3.3V and out pin 13 at 5V) to the anode of DA04 causes the same results.

### **MONITOR MUTE PATH: Shown going to the Terminal PWB. Labeled as V MUTE 2:**

The high from Q440 is routed to PST2 pin 9. On the terminal board is an exact same circuit as describe in the Out to Hi-Fi Mute Path above. So the actual circuit is not show here, just the description. The high from the PST2 connector is then sent to the anode of DX03. Then to DX01, and DX02 fire and supply the high to the bases of QX01 and QX02. These in turn ground out the audio to the Monitor Out jacks.

Also, the high from the Microprocessor pin 49 to I007 (in pin 3 at 3.3V and out pin 17 at 5V) to the same circuit.

### **CRT MUTE PATH: Shown going to the CRT PWB. Labeled as V MUTE 1:**

The high from Q440 is routed to PSC pin 11. This high goes to Q8C1 base. This turns on and supplies a ground to the following diodes, D8A3 on the Blue CRT PWB, D853 on the Green CRT PWB, D803 on the Red CRT PWB. When the diodes are supplied with a ground on their cathodes, they remove the base voltage fro the RGB drivers, Q8A3, Q853, and Q803 on the Blue, Green and Red CRT PWBs.

### **FRONT AUDIO OUT HARD MUTE PATH: Labeled as V MUTE 2:**

The high from Q440 is routed to DA08. The high continues to the base of QA11. When this transistor turns on, it supplies a Lo to pin 11 of IA03 and hard mutes the Audio Out. (Note: This is not the same thing as the Mute selected from the customer's remote. This is supplied by the Front Audio Control IC and functions in three states, No Mute = 100%, 1/2 Mute = 50% and Full Mute = 0%. Also, the high from the Microprocessor pin 49 to I007 (in pin 3 at 3.3V and out pin 17 at 5V) to the same circuit.

### **FRONT AUDIO OUT MUTE and A MUTE PATH: Labeled as V MUTE 2 and A MUTE:**

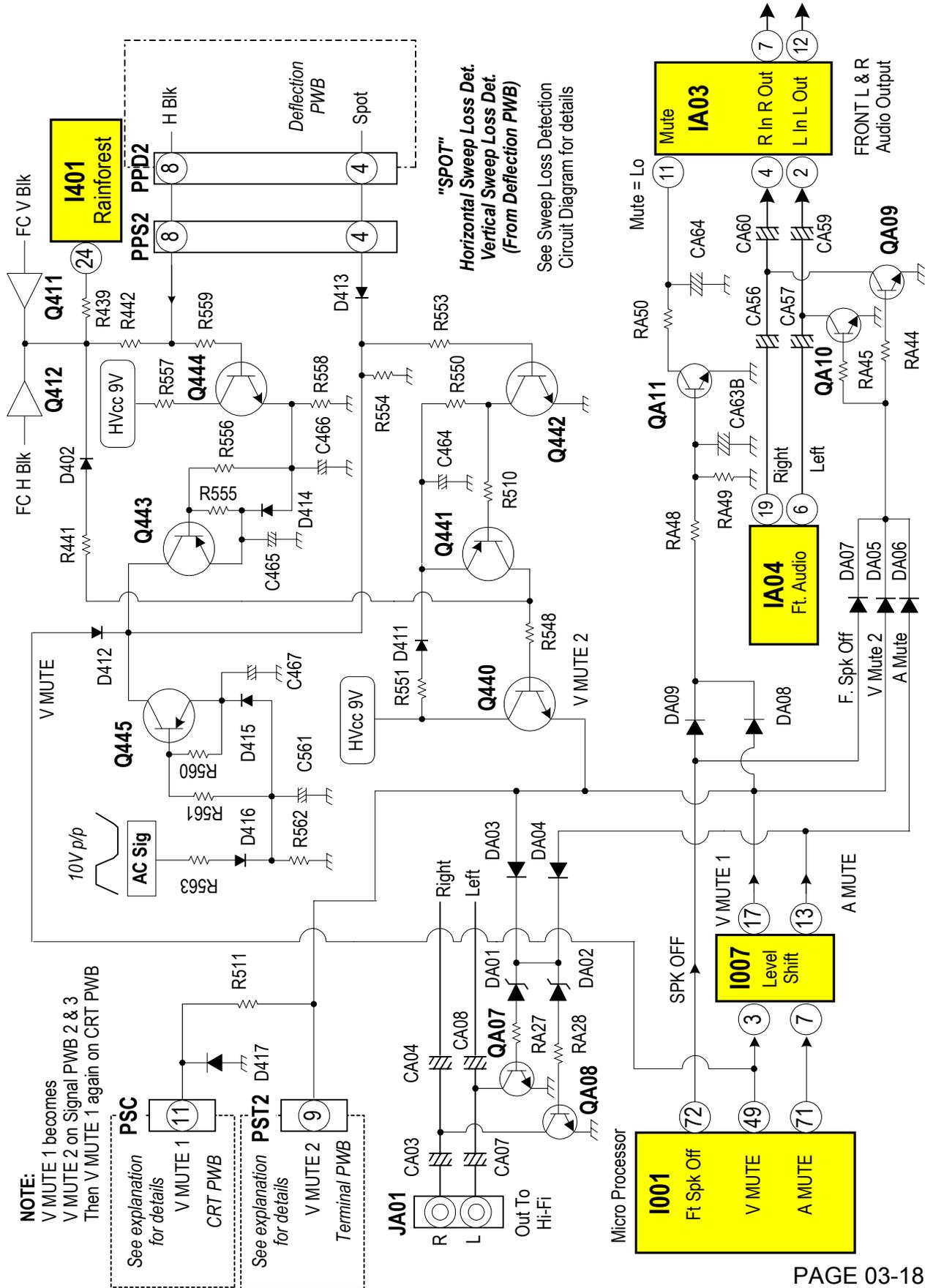
The high from Q440 is routed to DA05. The high continues to the base of QA19, and QA10.

When these transistor turns on, they in turn ground out the audio going into the Audio Output IC, Right audio in pin 4 of IA03, Left audio in pin 2 of IA03

**A MUTE:** Also, the high from the Microprocessor pin 71 to I007 (in pin 7 at 3.3V and out pin 13 at 5V) to the anode of DA06 and on to the same circuit.

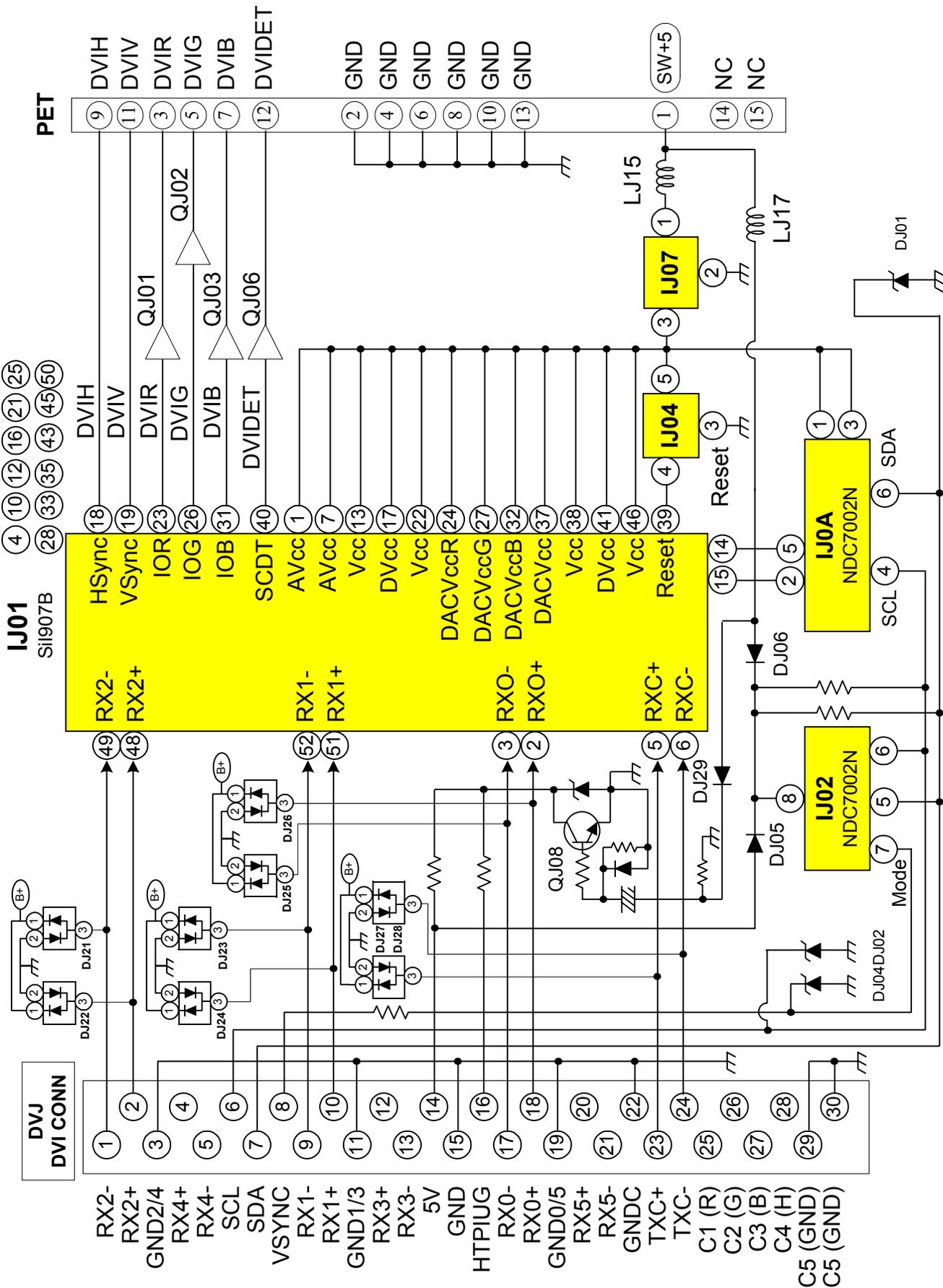
**Ft Spk Off: (Front Speaker Off)** Also, the high from the Microprocessor pin 72 to the anode of DA07 and on to the same circuit.

# DP-2X Series Chassis AUDIO and VIDEO MUTE Circuit



# DP-23, DP-23G, DP-26, DP-27 and DP-27D CHASSIS DVI SIGNAL PATH (Not DP-24)

All of these pins are ground



## DP-2X COMPONENT SYNC CIRCUIT EXPLANATION

*(See DP-2X Series Chassis Main/Component Sync Separation Signal Path for details)*

This diagram shows the route for sync utilized when the set has selected Component inputs.

### **IX02 Main Y Pr/Pb Selector:**

The Component inputs are Component 1 at pin **59** and Component 2 at pin **5**. The Y component for NTSC is input at pin **53**.

### **Main Y Output from IX02:**

The Y component from the selected source is output at pin **44**. Then through **QX22** to the Main Video Chroma Y Pr/Pb Switch **IZ02** pin **30** and pin **6**. After internal separation, the H Sync is output at pin **17** and the V. Sync is output at pin **15**.

### **H. Sync from IZ02 pin 17:**

This is routed through the transistor **QZ14** then to the connector **PST1** pin **1**. From here it is split. One route is into the **PFC1** pin **8** connector on the Flex Converter **U303** called M H In (Main Horizontal In). The Flex Converter uses this signal for a timing signal as it performs it's conversions.

The other route from the **PST1** connector pin **1** is to pin **13** of the Sync selector IC **I402**. If the control line at pin **11** is high, this H. Sync is routed out pin **14** to pin **16** of the Rainforest IC **I401**. This sync is used if the set is receiving a true 1080i signal and the Flex Converter is bypassed.

### **V. Sync from IZ02 pin 15:**

This is routed through the transistor **QZ18** then to the connector **PST1** pin **2**. From here into the **PFC1** connector pin **7** on the **Flex Converter U303** called M V In (Main Vertical In). The Flex Converter uses this signal for a timing signal as it performs it's conversions.

### **PinP (Sub) Y Output from IX01:**

The Y component from the selected source is output at pin **50**. Then through **QX19** to the Sub Video Chroma Y Pr/Pb Switch **IZ01** pin **30** and pin **6**. After internal separation, the H Sync is output at pin **17** and the V. Sync is output at pin **15**.

### **H. Sync from IZ01 pin 17:**

This is routed through the transistor **QZ13** then to the connector **PST2** pin **28**. From here it is routed into the **PFC1** pin **15** connector on the Flex Converter **U303** called S H In (Sub Horizontal In). The Flex Converter uses this signal for a timing signal as it performs it's conversions.

### **V. Sync from IZ01 pin 15:**

This is routed through the transistor **QZ15** then to the connector **PST2** pin **29**. From here into the **PFC1** connector pin **14** on the **Flex Converter U303** called S V In (Sub Vertical In). The Flex Converter uses this signal for a timing signal as it performs it's conversions.

### **I402 Sync Selector to the Rainforest IC I401:**

One route for the H. Sync for the Main Picture is from the **PST1** connector pin **1** is to pin **13** of the Sync selector IC **I402**. If the control line at pin **11** is high, this H. Sync is routed out pin **14** to pin **16** of the Rainforest IC **I401**. This sync is used if the set is receiving a true 1080i signal and the Flex Converter is bypassed.

The other route is for Horizontal Sync from the Flex Converter **U303** pin **7** of **PFC2**. This Horizontal Sync signal is called HD Out (Horizontal Digital Output, meaning that the signal has gone through the Digital manipulation within the Flex Converter). This signal is routed to pin **12** of **I402**. If the control line at pin **11** is Low, this H. Sync is routed out pin **14** to pin **16** of the Rainforest IC **I401**. This sync is used if the set is using a signal that has been processed by the Flex Converter.

### **Vertical Sync from the Flex Converter U303 to the Rainforest IC I401:**

The other route is for Vertical Sync from the Flex Converter **U303** pin **6** of **PFC2**. This Vertical Sync signal is called VD Out (Vertical Digital Output, meaning that the signal has gone through the Digital manipulation within the Flex Converter). This signal is routed to pin **15** of the Rainforest IC **I401**. This sync is used no matter what source, because all vertical timing is the same.



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# **AUDIO INFORMATION**

**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 4**

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## DP-2X AUDIO CIRCUIT EXPLANATION

*(See DP-2X Chassis Audio (Main-Terminal) Signal Path for details)*

### IX01 AUDIO VIDEO SELECTOR IC:

The main Audio path is delivered to the Audio/Video Selector IC **IX01** to the following pins;

**62 (Left) and 64 (Right):** This is the Audio input from the Main Tuner **U301**. The integrated Tuner has an Internal Audio decoding circuit that outputs Lt (Left Total) from pin **26** and Rt (Right Total) from pin **27**. The Left continues through the **PST1** connector pin **21** and the Right continues to pin **20**. They arrive at **IX01** pins **62** and **64** respectively.

**2 (DM-Left) and 4 (DM-Right):** This is the Audio input from the ATSC Tuner **UD2002**. The Digital Tuner has an Internal Audio decoding circuit that outputs Lt (Left Total) from pin **10** and Rt (Right Total) from pin **9**. The Left continues through the **PST1** connector pin **25** and the Right continues to pin **26**. They arrive at **IX01** pins **2** and **4** respectively. The Digital Module (ATSC Tuner) is only available on the DP-26 chassis).

**59 (Left) and 61 (Right):** This is the Audio input from Auxiliary 1 input. This audio is associated with component input 1 and with DVI input. (DVI is not available on the DP-24 chassis).

**29 (Left) and 31 (Right):** This is the Audio input from Auxiliary 2 input. This audio is associated with component input 2 which also accepts composite video on the Y jack.

**16 (Left) and 18 (Right):** This is the Audio input from Auxiliary 3 input, composite or S-In only.

**9 (Left) and 10 (Right):** This is the Audio input from Auxiliary 4 input, composite or S-In only.

**23 (Left) and 25 (Right):** This is the Audio input from the front Auxiliary 5 input, composite or S-In only. These inputs are delivered through the **PFT** connector pins **4** and **5** respectively.

### MONITOR OUTPUTS:

**38 (Left) and 40 (Right):** This is the Monitor Audio Outputs.

### LEFT and RIGHT OUTPUTS:

**43 (Left) and 35 (Right):** This is the Left Total and Right Total output which represent the Audio associated with the Main picture. The Lt and Rt represent the fact that the Audio has any Dolby ® encoding still embedded.

The outputs are then routed through the **PST1** connector pins **10 (Left) and 9 (Right)** to the Center Select IC **I005** pins **2** and **12** respectively. **I005** is responsible for selecting the audio input from the Center Jack when the customer has set the television to operate in TV as Center Mode. The Center audio is routed to pins **1** and **13**. The control switching signal is provided by the Microprocessor **I001** pin **61** through the inverter **QA16** to pin **10** and **11**. A low on these pins with switch to receive inputs from the main L and R and a high on these pins will place the IC into the Center mode.

The audio from **I005** leaves pin **15** Left and **14** Right and into the Audio Control IC **IA01**.

### IA01 AUDIO CONTROL IC:

This IC is responsible for controlling the audio Surround formats as well as volume, bass, balance, treble and customer mute. The Microprocessor outputs I2C bus control lines from pin **28 (SCL)** and **31 (SDA)** to pin **14** and **13** respectively. Dependant upon the Surround mode selected the audio is interfaced with **IA02** which acts as the **BBE/SRS** IC. The control pins for IA02 are listed in the table to the right.

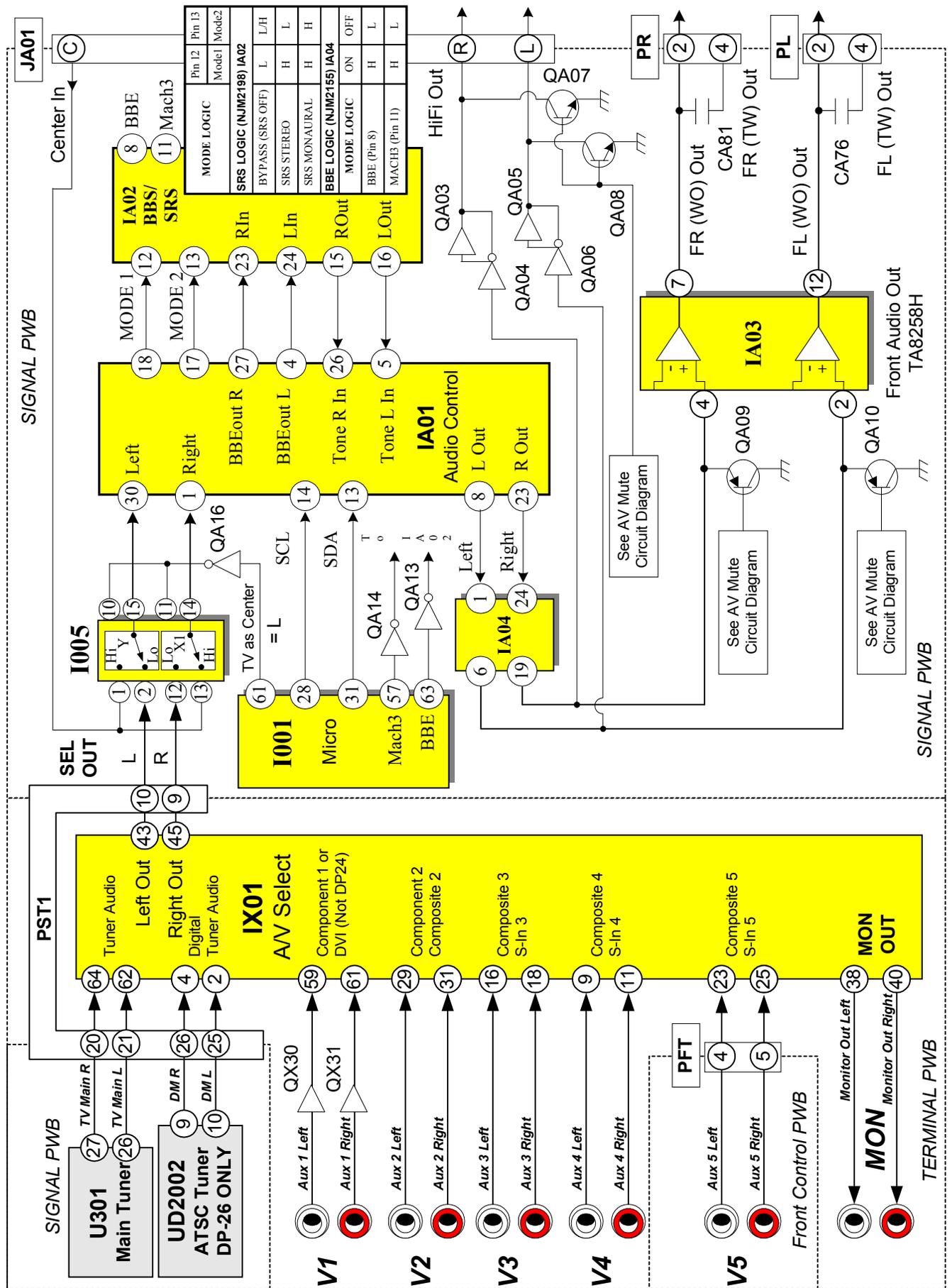
The Audio is output from pin **8 (L)** and **23 (R)** to **IA04** which buffers the audio and outputs on pin **6 (L)** and **19 (R)** to two different circuits. Primary route is to the Audio Output IC **IA03** pins **2 (L)** and **4 (R)** and out pin **12 (L)** and **7 (R)** to the speaker plugs **PL** and **PR**.

The Secondary route from **IA04** is to the Out to Hi-Fi jacks.

*(See the Audio Video Mute circuit for details on the Mute transistors operation and control).*

MODE LOGIC	Pin 12	Pin 13
	Mode1	Mode2
<b>SRS LOGIC (NJM2198) IA02</b>		
BYPASS (SRS OFF)	L	L/H
SRS STEREO	H	L
SRS MONAURAL	H	H
<b>BBE LOGIC (NJM2155) IA04</b>		
MODE LOGIC	ON	OFF
BBE (Pin 8)	H	L
MACH3 (Pin 11)	H	L

# DP-2X Chassis Audio (Main-Terminal) Signal Path



# **DEFLECTION INFORMATION**

**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 5**

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## DP-2X HORIZONTAL DRIVE CIRCUIT EXPLANATION

### HORIZONTAL DRIVE CIRCUIT DIAGRAM DESCRIPTION:

*(Use the DP-2X Horizontal Drive Circuit Diagram for details)*

### CIRCUIT DESCRIPTION

When B+ arrives at the Rainforest IC **I401** pin (19), horizontal drive is output from pin (26). The drive signal is routed through the connector **PSS2, PPD2** pin 8 to the Horizontal Driver Transistor **Q709**. This transistor switches the ground return for pin (8) of the Driver transformer (**T702**). **SW+28** volts is supplied to pin (5) and this switching allows EMF to develop. As this signal collapses, it creates a pulse on the output pin of (**T702**) at pin (4) to the base of the Deflection Horizontal output transistor **Q777**. This transistor provides primary switching pulses for the Deflection Transformer **T701**.

### Q777 TRANSISTOR PRODUCES THE FOLLOWING OUTPUT PULSES;

1. The **Dynamic Focus OUT Circuit to QF01**: A Dynamic Focus waveform, (Horz. Parabola) is created. This is a parabolic waveform that is superimposed upon the static focus voltage to compensate for beam shape abnormalities which occur on the outside edges of the screen because the beam has to travel further to those locations.
2. **Horizontal Deflection Yokes drive signals**. The collector of **Q777** provides the drive signal for all Horizontal Deflection Yokes.

### T701 TRANSFORMER PRODUCES THE FOLLOWING OUTPUT PULSES;

- **Deflection H. Pulse from pin (7)**: This pulse is used by;

### HORIZONTAL BLANKING (H. BLK) GENERATED FROM PIN (7):

The Horizontal Pulse is also routed to the Horizontal Blanking generation transistor **Q706**. This transistor generates the 13V P/P called **H Blk**. This signal goes to the following circuits;

- To the **PPD2, PPD2** connector pin 8 to pin (24) of **I401** as **FBP In**. Here this signal is used as a comparison signal. It is compared to the reference signal coming in at pin (16) Horizontal Sync. If there are any differences between these two signals, the output Drive signal from pin (26) is corrected.  
**NOTE**: When a 1080i signal is input through component inputs, the Rainforest IC detects this as well and outputs the ABL Switch signal from pin (36). *(See ABL Switch Circuit Diagram for details)*. The Reference signal for Horizontal Sync now becomes the Y input from component, pin (8).
- The H Blk signal is routed from here to the the Microprocessor which uses this signal for OSD positioning and for Station Detection during Auto programming within the coincidence detector, also as a detection signal to activate the AFC Loop.  
The PinP unit uses this signal for switching purposes. Like the read/write clock, positioning, etc...
- Through the **PDG** connector pin 14 to the Convergence circuit for correction waveform generation.
- Through **CN01** to the Sweep Loss Circuit (**QN01**) to shut off the drive to the CRTs if Horizontal deflection is lost.

### HORIZONTAL DRIVE FOR THE HIGH VOLTAGE:

- The Horizontal Blanking signal **H Blk** from **Q706** is also sent to the High Voltage Driver IC **IH01** pin (3). This IC uses this signal as its reference signal to produce the High Voltage Drive waveform output from pin (1). This output is routed to the driver transistors, **QH02**. Then to the High Voltage Horizontal Output Transistor **QH01**. This transistor switches the primary of the Flyback transformer **TH01**. Deflection SW +115 is sent through pin (9) and output pin (10) to the collector of the Horizontal Output Transistor **QH01**.

A sample of the High Voltage is output from the Flyback transformer **TH01** pin (12). This voltage is sent to pin (9) of the High Voltage Driver IC **IH01**. This voltage is compared to the reference voltage available at pin (12).

*(Continued on page 2)*

## DP-2X HORIZONTAL DRIVE CIRCUIT EXPLANATION

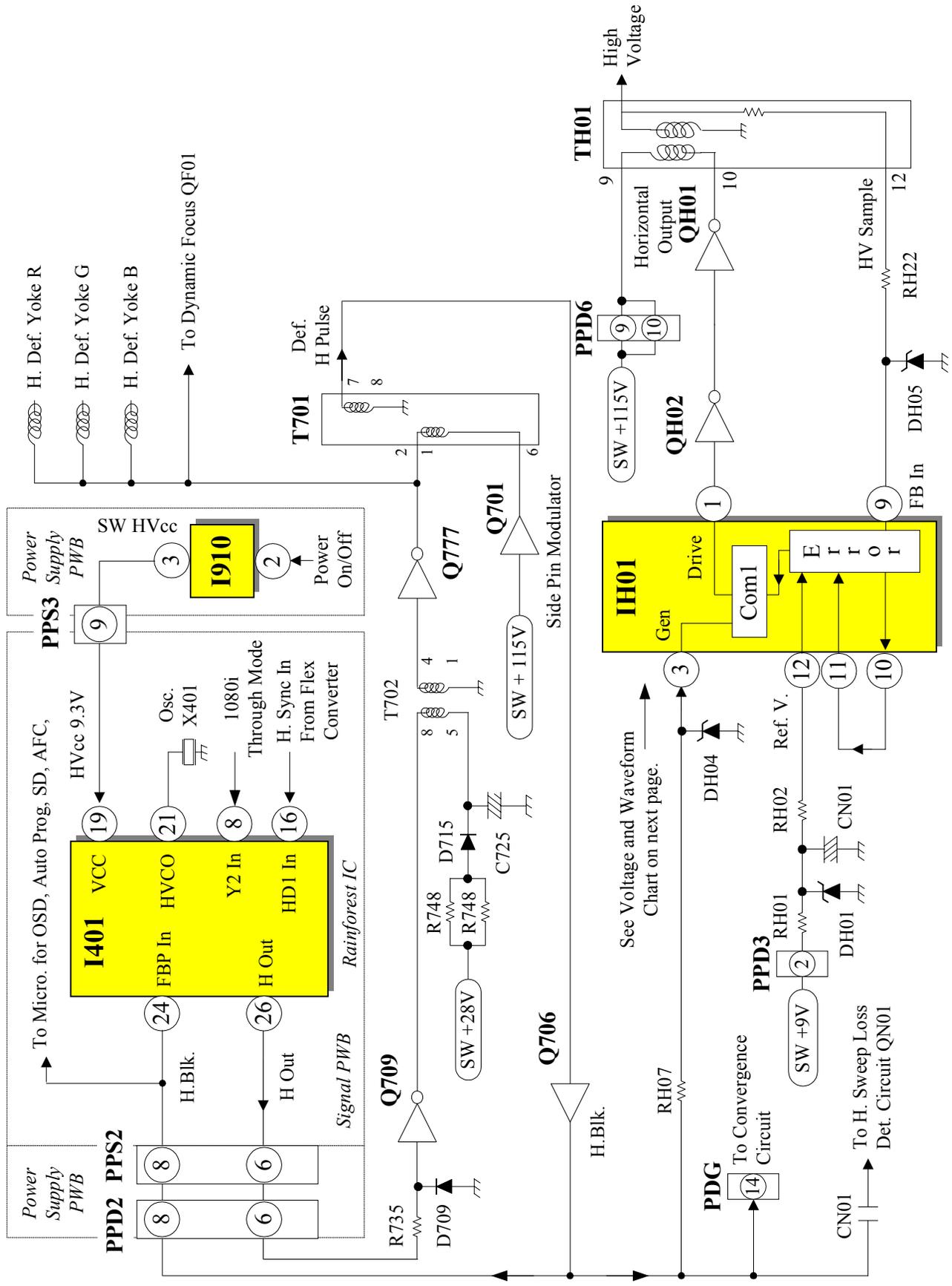
If there is a difference between the two voltages, an error voltage is generated and output from pin (10) and input again at pin (11) where it manipulates the PWM (Pulse With Modulation) signal producing the Horizontal Drive signal output from pin (1).

It's important to notice that the High Voltage circuit can not function without the Horizontal Deflection circuit providing a drive signal.

### ***GENERAL INFORMATION:***

The DP-2X deflection circuit differs from analog Hitachi projection televisions. It utilizes in a sense, two horizontal output circuits. One for Deflection and one for High Voltage. This allows for better deflection stabilization and is not influenced by fluctuations of the High Voltage circuit which may cause unacceptable breathing and side pulling of the deflection.

# DP-2X SERIES CHASSIS HORIZONTAL DRIVE CIRCUIT



## DP-2X IH01 HIGH VOLTAGE DRIVER IC WAVEFORM AND VOLTAGES

### IH01 NORMAL OPERATION:

Pin 1 = 6.80V with Color Bar,  
Varies with Brightness levels.

Pin 2 = 11.72V

Pin 3 = 0.59V

Pin 4 = 2.47V

Pin 5 = 1.60V

Pin 6 = 10.58V

Pin 7 = 0.0V

Pin 8 = 0.0V

Pin 9 = 4.90V

Pin 10 = 0.03V

Pin 11 = 0.03V

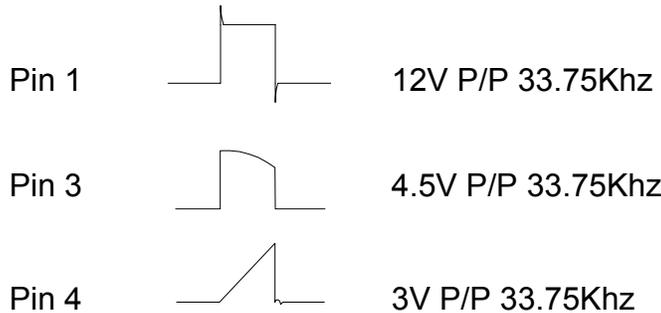
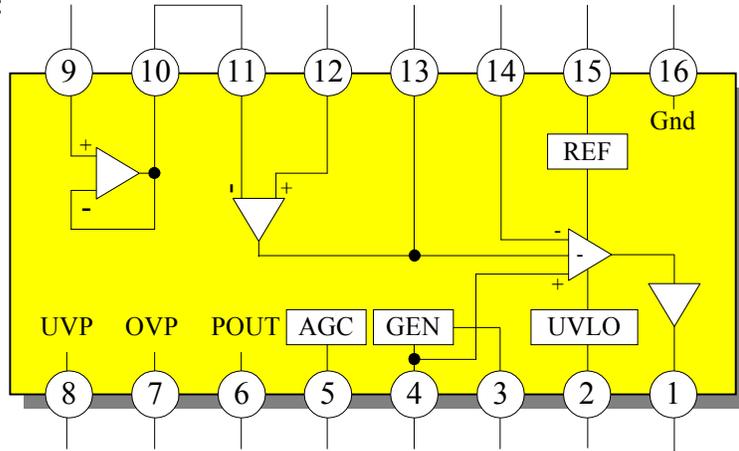
Pin 12 = 4.90V

Pin 13 = 0.05V

Pin 14 = 2.02V

Pin 15 = 4.96V

Pin 16 = 0.0V



### IH01 NOT RUNNING:

Pin 1 = 12.28V

Pin 2 = 11.86V

Pin 3 = 3.96V

Pin 4 = 3.5V

Pin 5 = 1.089V

Pin 6 = 0.021V

Pin 7 = 0.0V

Pin 8 = 0.0V

Pin 9 = 0.019V

Pin 10 = 0.038V

Pin 11 = 0.038V

Pin 12 = 4.90V

Pin 13 = 0.05V

Pin 14 = 4.59V

Pin 15 = 4.96V

Pin 16 = 0.0V

### NOT RUNNING EXPLANATION:

This situation can happen and possibly lead the Service Technician off on the wrong path.

Take a quick look at the voltages for pin 3 and 14. This is the key. These two pins tie back to the Horz. and Vert. Sweep Loss Detection Circuit.

*(See page 05-05 for the Sweep Loss Detection Circuit Diagram).*

If the Sweep Loss circuit is activated, it outputs a high from QN02.

This high is used to shut off the CRT to prevent CRT burn, However, the Collector of QN02 is also routed to these two pins through diodes DN09 to pin 14 and DN10 to pin 3.

When QN02 goes high, it drives pin 3 and 14 high which turns off the internal oscillator of IH01 via pin 3. This action stops Horizontal Drive to the High Voltage circuit. This action causes pin 1 to saturate and it goes High.

Note that pin 14 is tied to an internal op-amp (-) leg. This cause the output to stop. So no Horizontal Drive is allowed to pass to the output amp. connected to pin 1.

## DP-2X SWEEP LOSS DETECTION CIRCUIT EXPLANATION

*(See DP-2X Sweep Loss Detection Circuit for details)*

The key component in the Sweep Loss Detection circuit is **QN02**. This transistor is normally biased off. When the base becomes 0.6V below the emitter, it will be turned on, causing the SW +9V to be applied to two different circuits, the *Spot* circuit and the *High Voltage Drive* circuit.

### SPOT ACTIVATION CIRCUIT

When **QN02** is turned on, the SW +9V will be applied to the anode of **DN11**, forward biasing it. This voltage will then pass through **DN11**. It will then be clamped by **DN12**, and arrive at pin 4 of **PPD2**, **PPS2**. It will then be directed to the Signal PWB where it will pass through **D413** and activate the Video Mute circuitry **Q442** - **Q441**. This is done to prevent CRT burns. *(See DP-2X Audio Video Mute Circuit for details)*

A control (enable) circuit for SPOT is routed from pin 5 of **PPS2**, **PPD2** called "CUT OFF". This will activate when accessing certain adjustments parameters in the service mode; i.e. turning off vertical drive for making CRT drive or cut-off adjustments. When Vertical Drive is defeated, the Vertical Sweep loss circuit would activate. Cut Off is produced from the Microprocessor **I001** pin 47 and routed to **QN06** to "inhibit" the Spot line from activating and shutting off the CRTs.

### HIGH VOLTAGE DRIVE CIRCUIT

When **QN02** is turned on, the SW +9V will also be routed through **RN15** and **DN09** and applied to the High Voltage Drive IC **IH01** at pin 14. When this occurs, the IC will stop generating the drive signal that is used to produce High Voltage via **QH02**, the High Voltage Driver. Again, this is done to prevent CRT burn, especially during sweep loss.

This high is also routed through **RN16**, **DN10** to pin 3 of **IH01** which also kills the internal drive.

### CONCERNING QN02

There are several factors that can cause **QN02** to activate; loss of vertical or horizontal blanking.

#### Loss of Vertical Blanking (V Blk)

The Vertical pulse at the base of **QN05** switches **ON05** on and off at the vertical rate. This discharges **CN03** sufficiently enough to prevent the base of **QN04** from going high to turn it on and activate **QN02**.

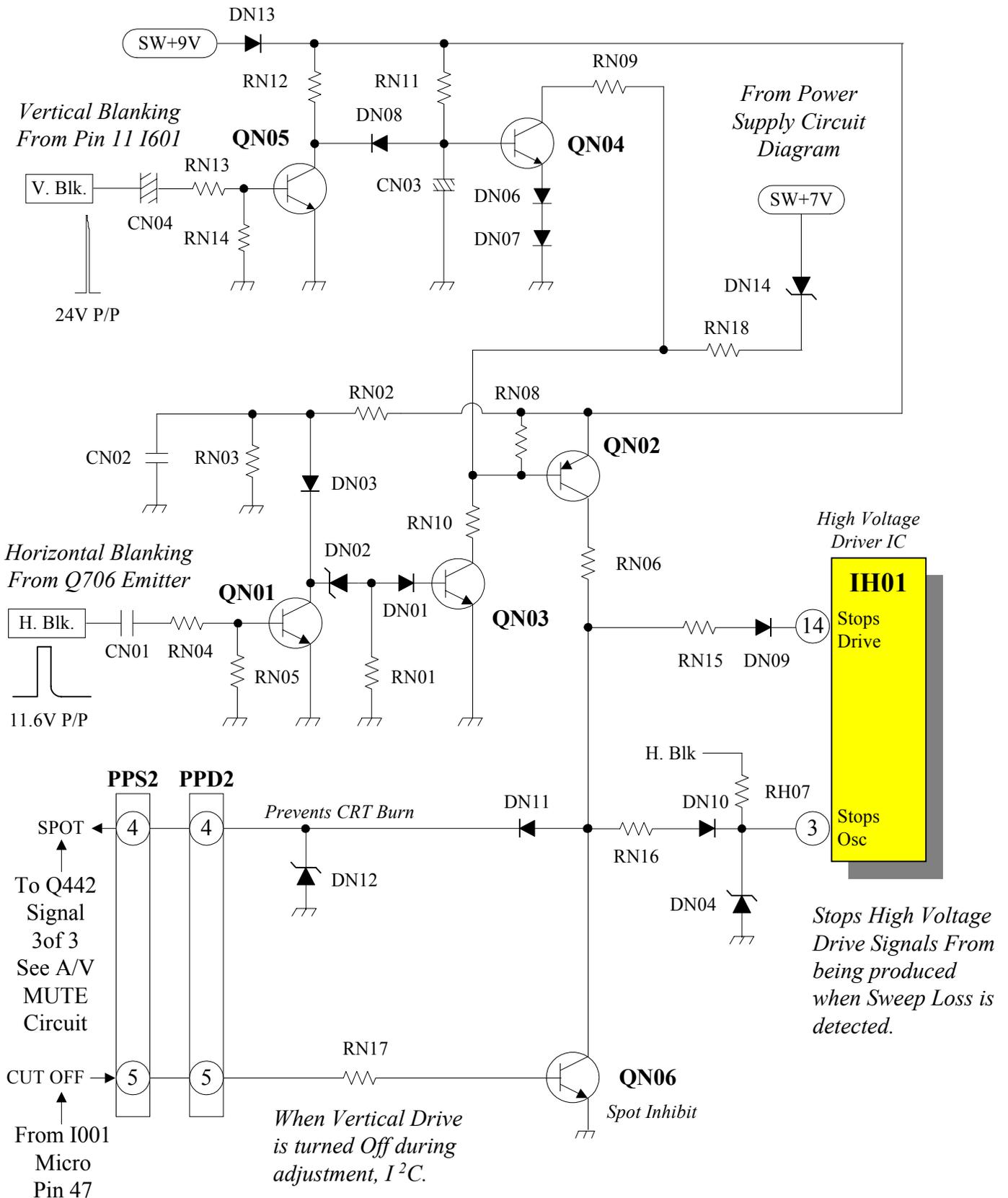
When the 24 Vp/p positive vertical blanking pulse is missing from **CN04** to the base of **QN05**, it will be turned off, which will cause the collector to pull up high because **CN03** charges up through **RN11**. This in turn will cause **QN04** to turn on because it's base pulls up high, creating an increase of current flow from emitter to collector and through **RN09**. **RN08**, (which is located across the emitter base junction of **QN02**), to the SW +9V supply. This increase of current flow through **RN08** will bias on **QN02** and the events described in "Spot Activation Circuit" above will occur.

#### Loss of Horizontal Blanking (H Blk)

The Horizontal pulse at the base of **QN01** switches **ON01** on and off at the horizontal rate. This discharges **CN02** sufficiently enough to prevent the base of **QN03** from going high to turn it on and activate **QN02**.

When the 11.6 Vp/p positive horizontal blanking pulse is missing from **CN01** to the base of **QN01**, it will be turned off, which will cause the collector to go high through **DN03**, **RN02** as the SW +9V charges **CN02**. This in turn will cause **QN03** to turn on because it's base is pulled up high when **DN02** fires. When **QN03** turns on, an increase of current flow from emitter to collector, through **RN10**, and up through **RN08**. This increase of current flow through **RN08** will bias on **QN02** and the events described in "Spot Activation Circuit" above will occur.

# DP-2X SWEEP LOSS DETECTION CIRCUIT



## DP-2X VERTICAL OUTPUT CIRCUIT EXPLANATION

*(See the DP-2X Series Chassis Vertical Output Circuit for details)*

### **I601 B+:**

The Vertical Output IC **I601** requires **SW+28V** to operate. This voltage is supplied from the Power Supply. The output for the **SW+28V** pulse is from pin **14** of **T902**. This power supply is protected by **E902**, rectified by **D918**, filtered by **C929, L913, C950** and output from the **PPD6** connector pin **1** and **2**. It arrives at the Deflection PWB and is routed through the Vertical B+ Excessive Current Sensor **R629, Q604** to pin **10** of **I601**.

### **TRIGGER PULSE:**

The Trigger pulse is routed from the Rainforest IC **I401** pin **27** on the Signal PWB. It is output from the **PPD2** connector pin **10**, through the Power Supply PWB and then through the **PPS2** connector pin **10** to the Deflection PWB. It is then sent to the Trigger Input on **I601** pin **3**.

During Trace, the internal Ramp Generator circuit using **C603** connected to pin **7** as the time constant begins charging. As it charges, the Pump Up circuit is also charging from the SW+28V to **C605**, through pin **11** to an internal switch of **I601**. When the Trigger pulse arrives (Retrace Time), the internal switch toggles over to the output stage push pull pair inside **I601**, and the +28V charged capacitor **C605** discharges. The output stage push pull pair inside **I601** already have +28V input from pin **10**. So the output pulse from pin **1** is now near 50V p/p. This is only needed for a short duration of time, (retrace) so the Charge Pump circuit eliminates the need for a 50V power supply.

### **(V BLK) VERTICAL BLANKING PULSE GENERATION:**

When the Charge Pump discharges and produces the 50V p/p pulse for Vertical drive during retrace, this pulse from pin **11** is also routed out as the Vertical Blanking pulse. Its amplitude is around 21V p/p and is sent to the following circuits;

- Vertical Sweep Loss detection circuit
- Convergence circuit for vertical correction waveform generation
- To the PPS2, PPD2 connector pin 12 to be sent to various circuits on the signal PWB. The Micro-processor uses this signal to time its OSD.

### **VERTICAL OUTPUT PULSE:**

The Vertical Output pulse is then routed to the Vertical Yokes generating a linear sawtooth current which moves the beam. (Trace = from top to bottom, Retrace = from bottom to top). This linear current is generated by the charge time constant of the vertical yokes charging **C607** through the low ohm resistors **R619, R620**.

### **VERTICAL YOKE CHARGE PULSE:**

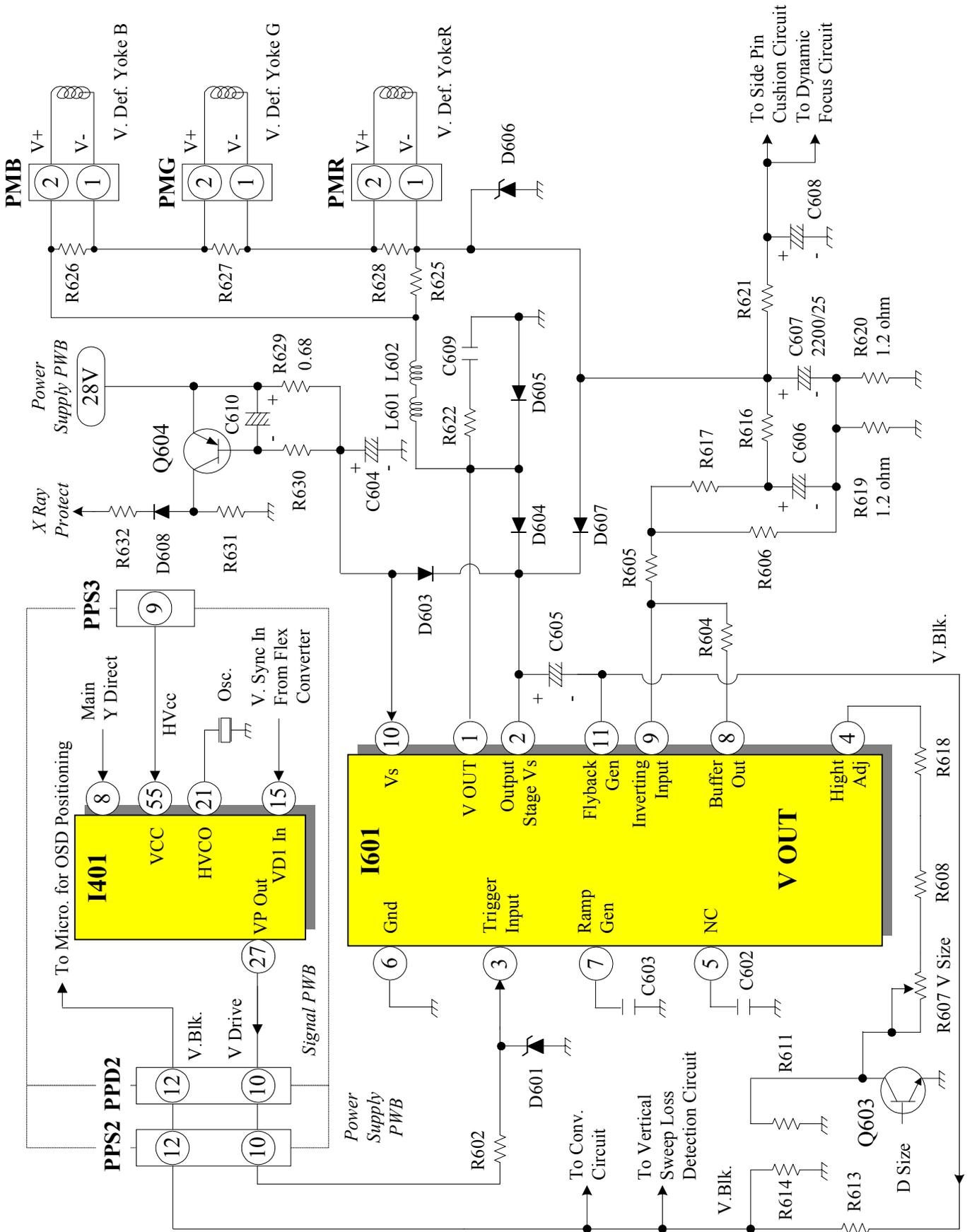
The pulse generated on the positive side of **C607** is also routed through the parabolic wave form generation circuit of **R621**, and **C608** to the side pincushion circuit and to the dynamic focus circuit for corrections to deflection and focus.

The pulse generated on the positive side of **C607** is also routed back to **I601** pin **8** and **9**. The AC component of this signal is for vertical linearity compensation. The DC component of this signal and the DC component provided by the Vertical size pot into pin **4** are routed back to the Ramp generator circuit described above. The DC component determines the charge time associated with the ramp generator or in other words, the Vertical height.

### **D SIZE SWITCH:**

When Magic Focus is activated by either the Magic Focus button or customer's menu or during service when the sensors are initialized, **Q603** receives the **D Size** command from the Digital Convergence Unit, **UKDG** pin 15 of **PDS** connector. When **Q603** turns on, it bypasses **R611** and lowers the resistance from **R607** (Vertical Size Pot) to ground. This increases the Vertical size to allow positive contact of the light pattern hitting the sensors.

# DP-2X SERIES CHASSIS VERTICAL OUTPUT CIRCUIT



## DP-2X SIDE PINCUSHION CIRCUIT EXPLANATION

*(See the DP-2X Side Pincushion Circuit for details)*

Due to the nature of deflection, the sides of the picture has a tendencies to pull in similar to an hour glass. The Side pincushion circuit is responsible for manipulating deflection to compensate. This is accomplished by super imposing a vertical parabolic waveform on the DC voltage utilized for Horizontal Size.

**VERTICAL YOKE CHARGE PULSE:** *(See Vertical Output Circuit for details)*

The pulse generated on the positive side of **C607** is routed through the parabolic wave form generation circuit of **R621**, and **C608** to the side pincushion circuit.

**SIDE PIN WAVE FORM GENERATION IC:**

Then through **R742**, **C702**, **R709** to pin **6** of **I701**. This is the positive leg of the internal op-amp. Also attached to this input circuit is the Horizontal Size circuit comprised of **R710**, **R711**, **R713** and clamped by **D714**. The variable resistor **R711** which adjust the DC level at pin **6**. The negative leg of the op-amp is connected through pin **5** to the feedback circuit from the Side Pin Cushion output circuit for stability.

The output of the DC offset voltage with Vertical parabolic wave form attached is then routed out pin **7** to the base of **Q703**. This transistor has it's emitter off set above ground by **D713**, **R747** back to the SW +9V and **R704**. This transistor drives the base of the Side Pin Cushion modulator transistor **Q701**. The collector of **Q701** is connected to the Deflection SW +115V. The DC offset voltage and Vertical parabolic side pin cushion compensation wave form is now super imposed on the SW +115V which is sent to the Deflection Transformer **T701** and the Horizontal Linearity circuit **C715**, **L703**, **R729** to the Horizontal Yoke returns.

**D SIZE SWITCH:**

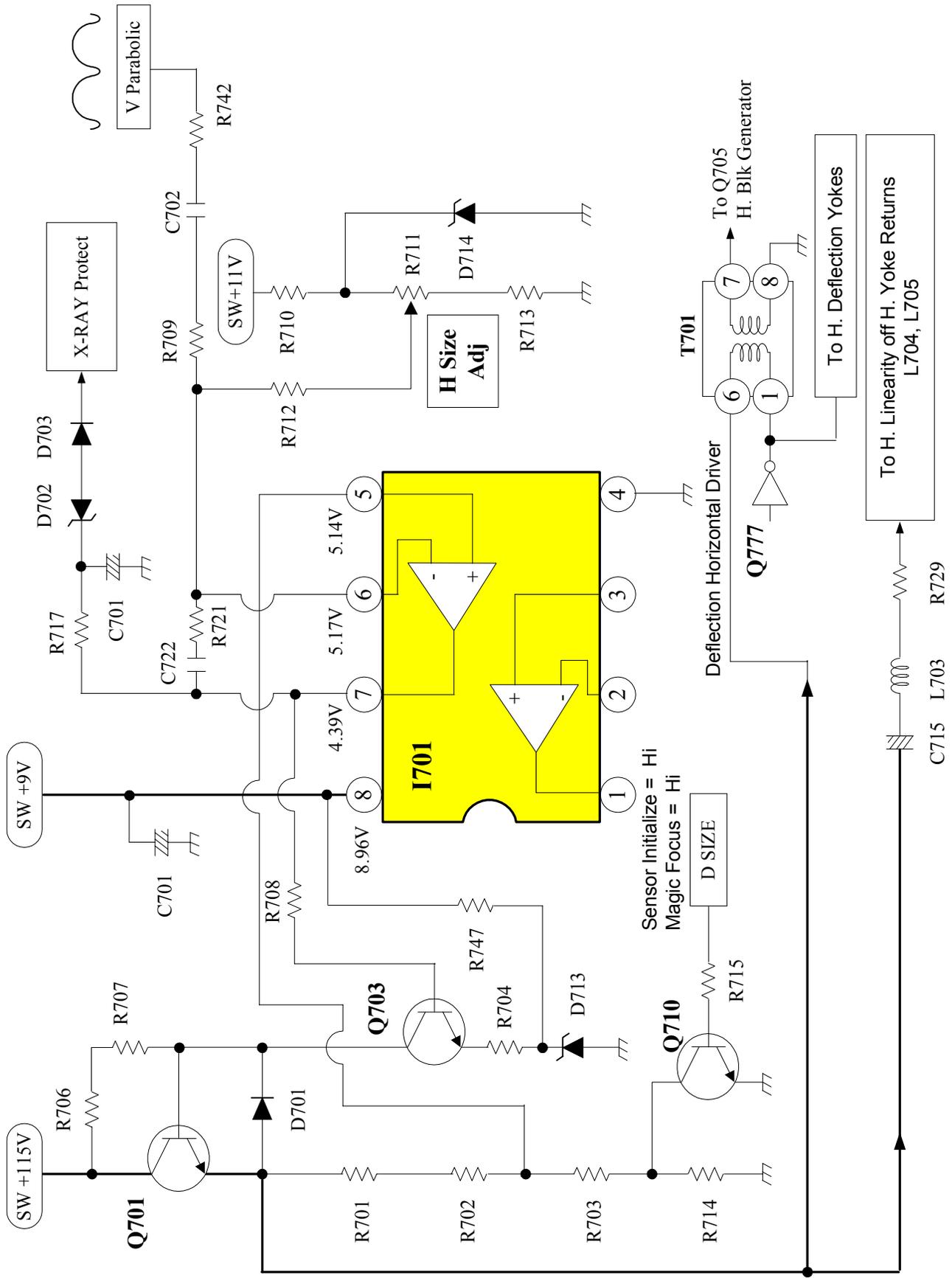
When Magic Focus is activated by either the Magic Focus button or customer's menu or during service when the sensors are initialized, **Q710** receives the **D Size** command from the Digital Convergence Unit, **UKDG** pin 15 of **PDS** connector. When **Q710** turns on, it bypasses **R714** and lowers the resistance from the emitter of **Q701** to ground. This increases the Horizontal size to allow positive contact of the light pattern hitting the sensors.

**X-RAY PROTECT:**

If something should fail within the Side Pincushion circuit that could cause a CRT burn, the voltage at pin **7** of **I701** is monitored by **D702**. If this zener fires because the voltage at it's cathode increases above a specified level, **D703** would forward bias and send a Shut Down command through the Protect line.

*(See Deflection Protect Power Supply Shut Down Circuit Diagram for details.)*

# DP-2X SIDE PINCUSHION CIRCUIT DIAGRAM



**DIGITAL  
CONVERGENCE  
INFORMATION**

**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 6**

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## DP-2X DIGITAL CONVERGENCE INTERFACE CIRCUIT EXPLANATION

data represents a specific correction signal for that specific location. When the Service Technician makes any adjustment, the new information must be stored in memory, EEPROM. The EEPROM only stores the 117 different adjustment points data, the SRAM interpolates to come up the additional 139 adjustment points for a total of 256 per color. The EEPROM data is slow in relationship to the actual deflection raster change. The SRAM is a very fast memory. So, during the first application of AC power, the EEPROM data is read and the SRAM makes the interpolation and as long as power remains, interpolation no longer has to be made.

This can be seen during an adjustment. If the Interpolation key is pressed on the remote control, what is happening is that the SRAM must make those additional calculations beyond the 117 made by the Servicer and this is all placed into memory.

### ***INFRARED REMOTE CONTROL INPUT SHOWN IN FIGURE 1:***

As can be seen in Figure 1, the Infrared Remote control signals actually manipulate the internal data when the Service Only Switch is pressed on the Deflection PWB. This process actually prevents the Microprocessor from responding to Remote commands, via a Busy line output from the DCU.

### ***INTERNAL CONTROLLER, D/A CONVERTERS SHOWN IN FIGURE 1:***

The internal controller, takes the stored data and converts it to a complicated Convergence correction waveform for each color. The Data is converted through the D/A converter, 1st and 2nd sample and hold, the Low Pass Filter that smoothes out the parasitic harmonic pulses from the digital circuit and the output Clamp that fixes the DC offset level.

The DC offset voltage is adjusted by several things.

- **Raster Centering.** The Raster Centering adjustment actually moves the DC offset voltage for Horizontal and Vertical direction. This Offset voltage will move the entire raster Up or Down, Left or Right.

When a complete Digital Convergence procedure has been performed and the adjustment information stored in memory by pressing the **PIP Mode** button twice (2), it is mandatory to run Sensor Initialization.

*If Sensor Initialization is not performed, the set will not allow Magic Focus to operate. If the Magic Focus button is pressed, the screen will display an adjustment grid instead.*

This is done by pressing the **PIP-MODE** button on the remote once (1), then pressing the **PIP CH** button. This begins a preprogrammed generation of different light patterns. Magic Focus memory memorizes the characteristics of the light pattern produced by the digital convergence module. If a convergence touchup is required in the future, the customer simply presses the **Magic Focus** button on the front panel or activates it from the customer's menu and the set begins another preprogrammed production of different light patterns. This automated process duplicates the same light pattern it memorized from the initialization process, re-aligns the set to the memorized convergence condition. Note that this process is using "Light" as it's source. This is a better process than using waveforms or voltages as it is adjusting using the actual light pattern as see by the customer.

### ***"MAGIC FOCUS" SENSORS SHOWN ON FIGURE 1:***

This process is a joint effort between the digital convergence module and **8 Photo-sensors**, physically located on the middle edges of the cabinet and the centers of the top and bottom, just behind the screen. The physical placement of the sensors assures that they will not produce a shadow on the screen that can be seen by the customer.

Magic Focus is activated by pressing the Magic **button** inside the front control panel door or by the Customer's Menu. An on-screen graphic display pattern will be displayed to confirm that the automatic convergence mode (Magic Focus) has begun.

The digital convergence module produces different patterns for each CRT, and the sensors on the side of the cabinet pick up the transmitted light and generate a DC voltage. This voltage is sent to the DCU and converted to digital data and compared with the memorized sensor initialization data. Distinct patterns will be generated in each primary color. As the process continues, the digital module manipulates the convergence correction waveforms that it is producing to force the convergence back into the original memorized configuration.

When all cycles have been completed, the set will return to the original signal and the convergence will be corrected. In most cases, activating the Magic Focus will allow the set to correct itself, without further adjustments.

*(Continued on page 3)*

## DP-2X DIGITAL CONVERGENCE INTERFACE CIRCUIT EXPLANATION

### EXPLANATION OF THE DIGITAL CONVERGENCE INTERCONNECT DIAGRAM:

#### ***INFRARED RECEIVER:***

During normal operations, the **IR** receiver directs its signal to the Main Microprocessor where it interprets the incoming signal and performs a predefined set of operations. However, when the Service Only Switch is pressed, the Main Microprocessor must ignore remote control commands. Now the DCU receives these commands and interprets them accordingly. The Microprocessor is notified at pin **42** when the DCU begins its operation by the BUSY line. As long as the BUSY line is active, the Main Microprocessor ignores the **IR** signal.

**NOTE: All chassis but the DP-24 has two IR Receivers. This allows operations of remote from any angle.**

**NOTE: The DP-24 only has one IR Receiver.**

#### ***ON SCREEN DISPLAY PATH:***

##### MICROPROCESSOR SOURCE FOR OSD:

The On Screen Display signal path is shown with the normal OSD information such as Channel Numbers, Volume Graphic Bar, Main Menu, Service Menu, etc... sent from the Main Microprocessor pins **34**, **33** and **32** to the **Rainforest IC I401** pins **37**, **38** and **39**. These are positive going pulses, about 5 V p/p and about 3uS in length dependant upon their actual horizontal time for display.

##### DCU (Digital Convergence Unit P/N CS00591) SOURCE FOR OSD:

The DCU has to produce graphics as well. When the **Service Only** switch is pressed, the Main Microprocessor knows the DCU is Busy as described before. Now the On Screen Display path is from the DCU pins **22**, **21** and **20** to the **Rainforest IC I401** pins **33**, **34** and **35**.

The output for the DCU OSD characters is output through the **PPG** connector pins (**20 Dig Red**, **21 Dig Green** and **22 Dig Blue**). These are routed through their buffers (**QK06 Dig Red**, **QK07 Dig Green** and **QK08 Dig Blue**) to the **PPD1**, **PPS1** connector pins (**2 Dig Red**, **4 Dig Green** and **5 Dig Blue**). Then through their buffers, (**Q422 Dig Red**, **Q421 Dig Green** and **Q420 Dig Blue**). Then it arrives at the **Rainforest IC I401** at pins (**35 Dig Red**, **34 Dig Green** and **33 Dig Blue**). When a character pulse arrives at any of these pins, the internal color amp is saturated and the output is generated to the CRTs. Any combination for these inputs generates either the primary color Red, Green or Blue or the complementary color Red and Green which creates Yellow, Red and Blue which creates Magenta or Green and Blue which creates Cyan.

#### ***OUTPUT STKS:***

These are output amplifiers that take the correction waveforms generated by the DCU and amplify them to be used by the Convergence Yoke assemblies for each color.

RV is Red Vertical Convergence correction. Adjust the location either up or down for Red.

RH is Red Horizontal Convergence correction. Adjust the location either left or right for Red.

GV is Green Vertical Convergence correction. Adjust the location either up or down for Red.

GH is Green Horizontal Convergence correction. Adjust the location either left or right for Red.

BV is Blue Vertical Convergence correction. Adjust the location either up or down for Red.

BH is Blue Horizontal Convergence correction. Adjust the location either left or right for Red.

#### ***CONVERGENCE YOKES:***

Each CRT has a Deflection Yoke and a Convergence Yoke assembly. The Deflection manipulates the beam in accordance to the waveforms produced within the Horizontal Deflection circuit or the Vertical Deflection circuit. The Convergence Yoke assembly manipulates the Beam in accordance with the correction waveforms produced by the DCU.

#### ***MAGIC FOCUS SENSORS AND INTERFACE: (8 Sensor Array).***

Each of the eight photo cells, called solar batteries in the service manual, have their own amps which develop the DC potential produced by the photo cells. Each amp is routed through the **PDS1** connector and arrives at the **PDS** connector on the DCU where the DCU converts this DC voltage to Digital signals. These digital signals are used only when the Magic Focus Button is pressed and Magic Focus runs or during Initialization of the sensors.

(Continued on page 4)

## DP-2X DIGITAL CONVERGENCE INTERFACE CIRCUIT EXPLANATION

### **MICROPROCESSOR:**

The Microprocessor is only involved in the Digital Convergence circuit related to disabling IR (Infrared Remote Control Signals). When the DCU is put into the Digital Convergence Adjustment Mode (DCAM) or Magic Focus, the Microprocessor ignores IR pulses. This is accomplished by the **BUSY** signal from the DCU. The **BUSY** signal is routed from the DCU out the **PDG** connector pin **19**, to the **PDD1** connector pin **1**, then the **PPS1** connector pin **1** to the Microprocessor **I001** notifying that the DCU is busy.

### **RAINFOREST IC (Video Processor).**

The Rainforest IC, **I401** is only involved with the Digital Convergence circuit related to OSD and Velocity Modulation inhibit during Digital convergence OSD operation in which it inhibits the Luminance from the main video.

### **SERVICE ONLY SWITCH:**

The Service Only Switch is located just in front of the DCU on the Deflection PWB. If the front speaker grills are removed and the front access panel is opened, the switch will be on the far left hand side. When this button is pressed with the TV ON, the DCU enters the Digital Convergence Adjustment Mode.

If the button is pressed and held down with the TV OFF and the power button is pressed, the Digital Convergence RAM is cleared. This turns off any influence from the DCU related to beam deflection. Magnetic centering is performed in the mode as well as the ability to enter the 3X3, (9 adjustment points) mode.

### **MAGIC FOCUS SWITCH:**

- Located on the Front Control panel is the Magic Focus switch. When Magic Focus is activated by the customer pressing this switch, the DCU enters the "**MAGIC FOCUS**" adjustment mode described earlier.
- When the Customer presses the Magic Focus Switch, the low is sent to the Microprocessor **I001** pin **45**. The Microprocessor then communicates with **I007** pin **8** (Level Shift) and it outputs a low on pin **12** (Magic Sw). This low is routed through the **PPS1**, **PPD1** connector pin **6** to the DCU connector **PDS** pin **1**. This starts the Magic Focus function.
- Also the Magic Focus can be started from the Customer's Menu. When selected by the customer, the same communication is performed to **I007** (Level Shift) and a low is sent out pin **1** to the DCU to start Magic Focus.

### **CONVERGENCE MUTE:**

**IK02** is the convergence mute IC. When the +28V line collapses when power is turned off, it's possible that the output STKs could be damaged. To prevent this, **IK02** monitors the +28V line. If it falls too low, pin **3** will output a Mute signal to pin **21** of connector **PDS** on the Digital Convergence Unit.

### **DIGICON ADJUST:**

This year, the Digital convergence can be adjusted by the customer. This is accessed from the Video Menu and selecting Magic Focus. Under the Magic Focus menu, select Manual. (See below). They have access to the 117 adjustment points for Red and Blue. (Green is fixed as reference). However, if after adjusting using this process, the customer can no longer use Magic Focus as it will return the set to it's original condition.

Video

**Magic Focus**

Aligns the Red, Green, and Blue colors to correct for Magnet Influences.

Adjustment Mode

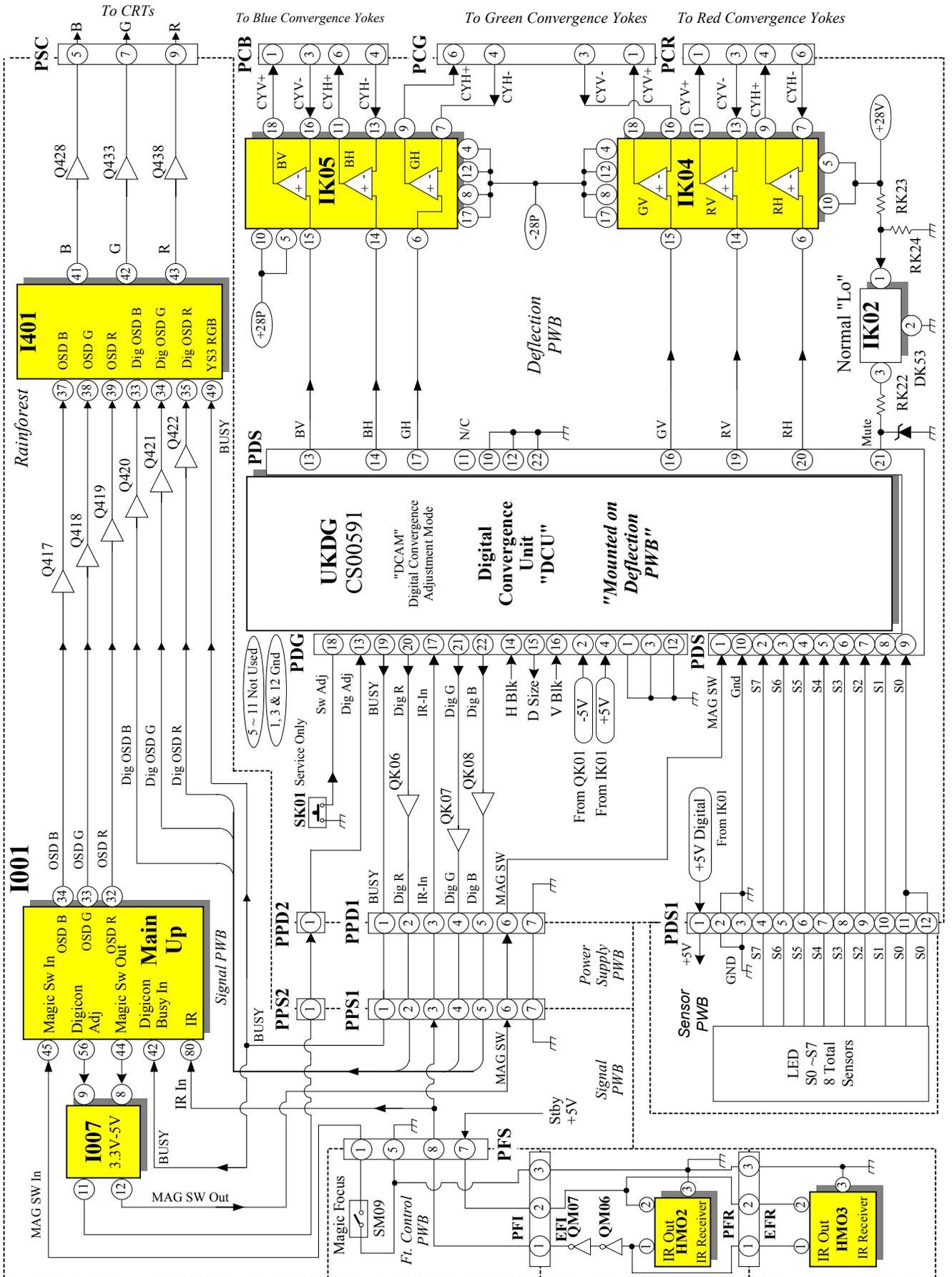
Auto

Manual

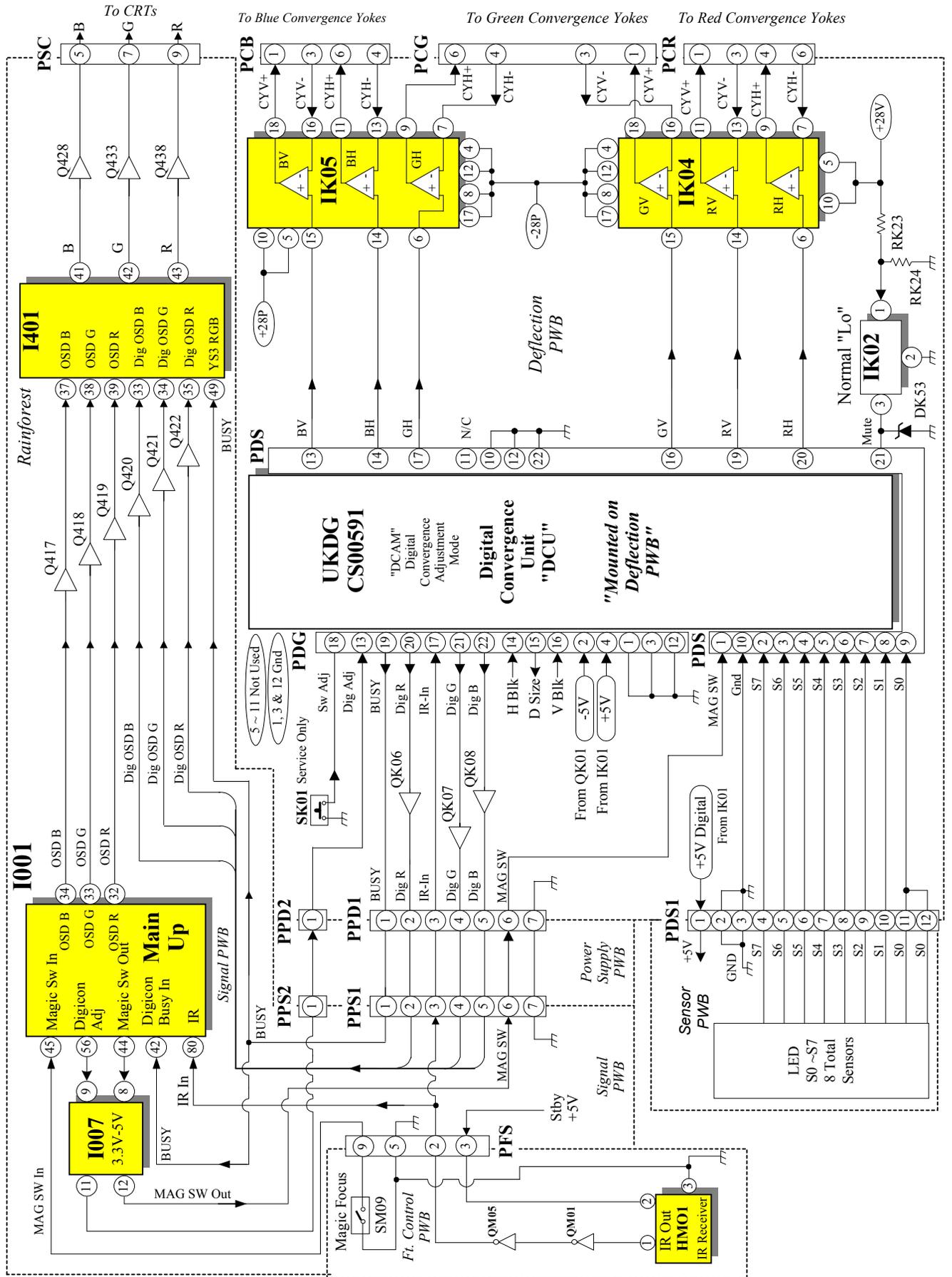
If you want to adjust now → **START**

▲ Move (Sel) Select

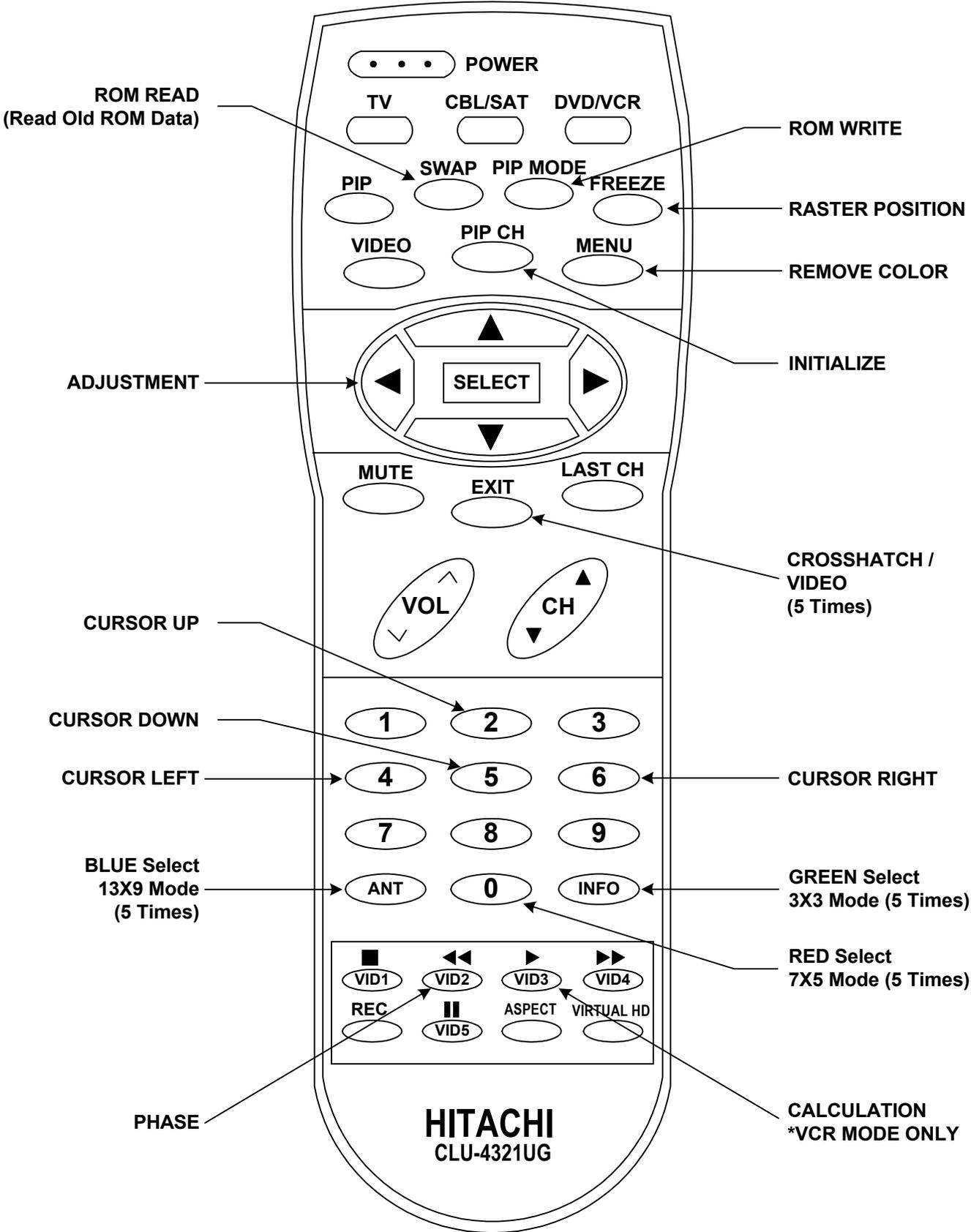
# DP-23, 23G, 26, 27 & 27D CHASSIS "DIGITAL CONVERGENCE" INTERCONNECTION CIRCUIT DIAGRAM



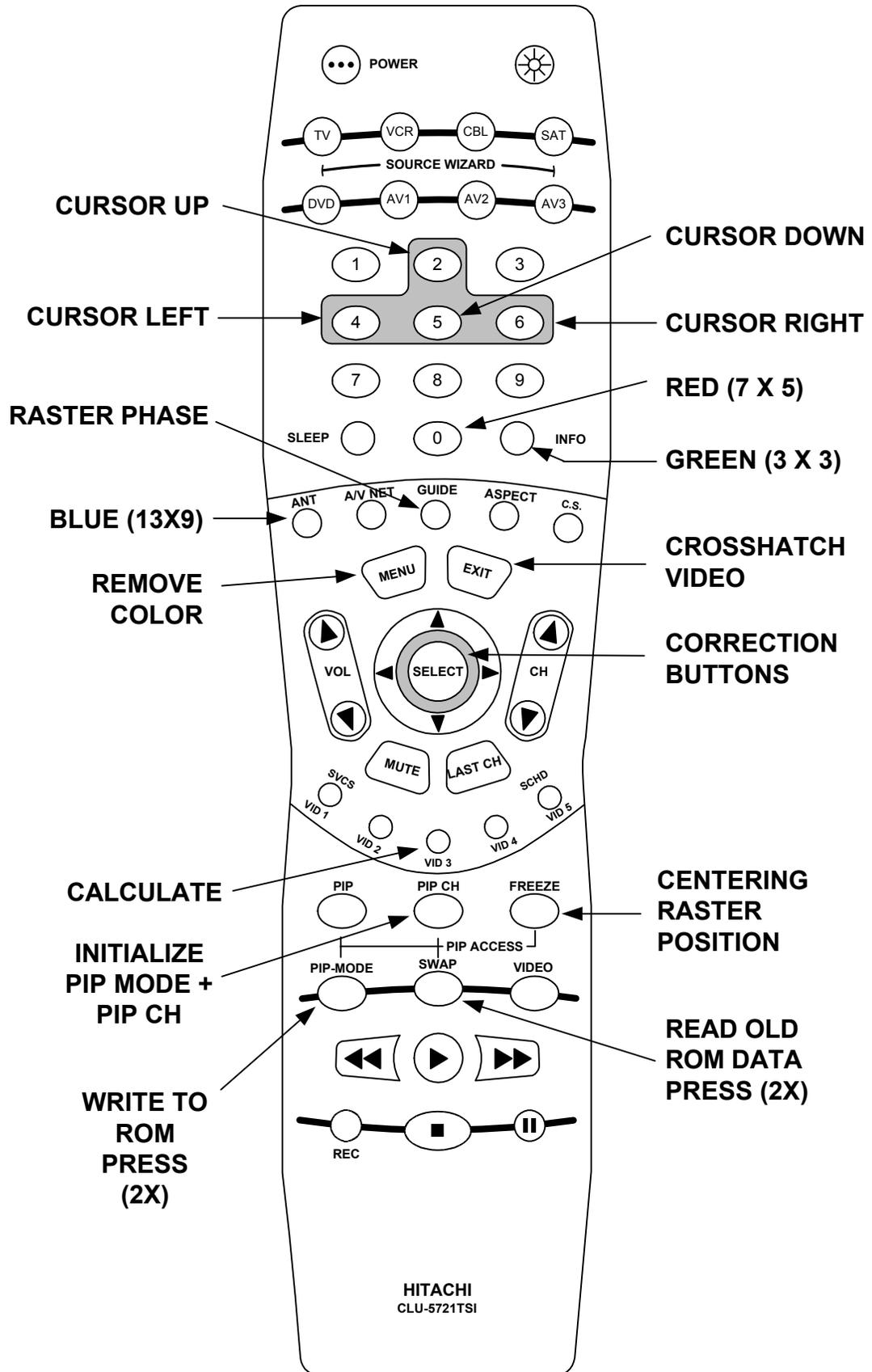
# DP-24 CHASSIS "DIGITAL CONVERGENCE" INTERCONNECTION CIRCUIT DIAGRAM



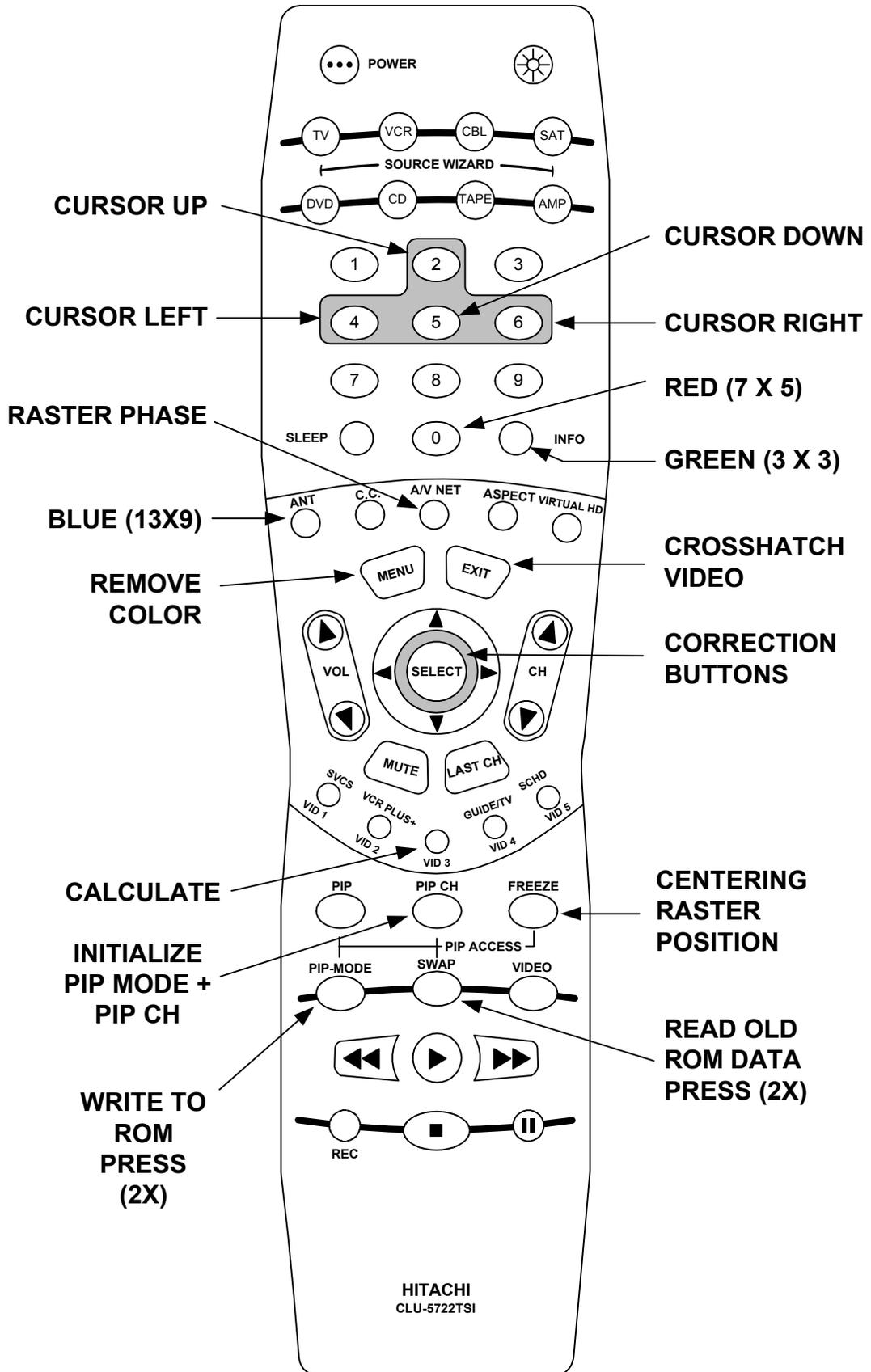
**DP-23, DP-23G & DP-24 REMOTE CONTROL CLU-4321UG  
(p/n HL01831)**



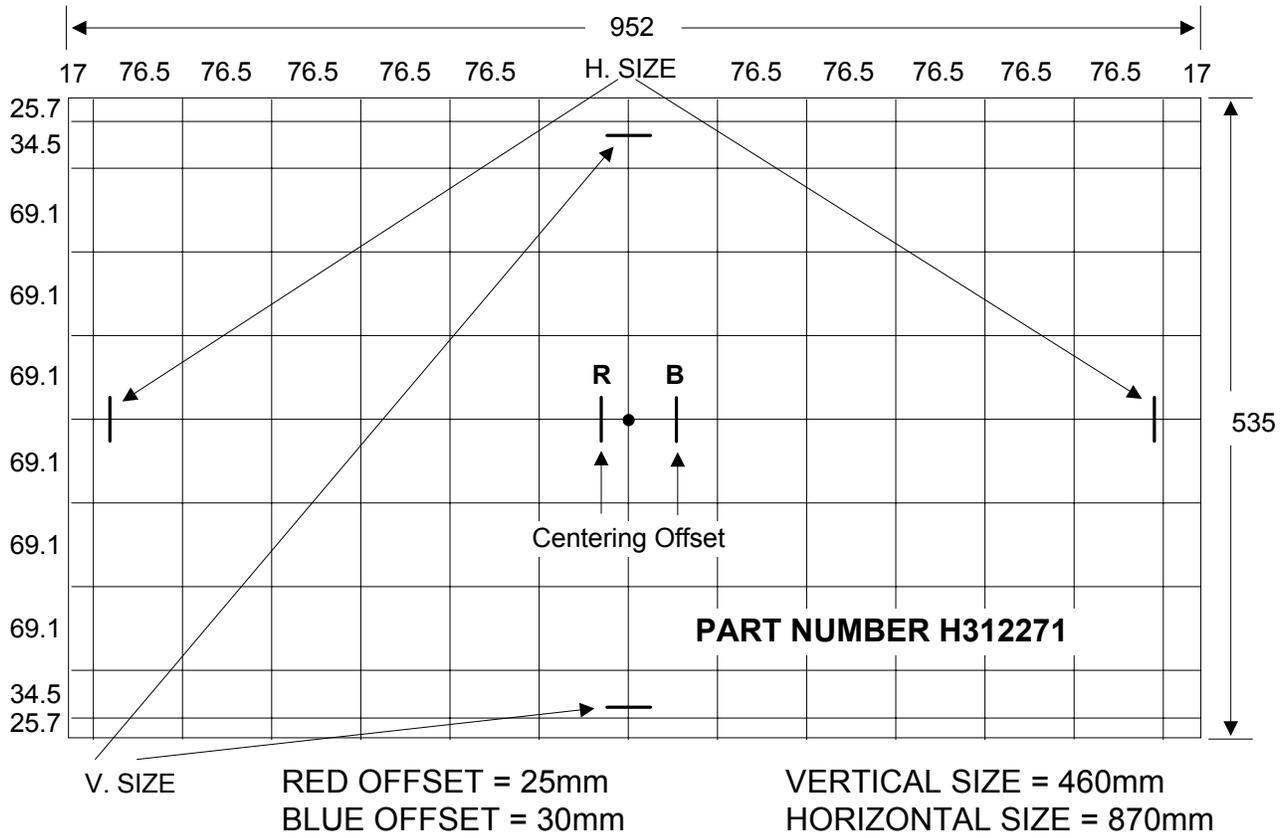
**DP-26 REMOTE CONTROL CLU-5721 TSI (P/N HL01821)**



**DP-27 & DP-27D REMOTE CONTROL CLU-5722 TSI (P/N HL01822)**

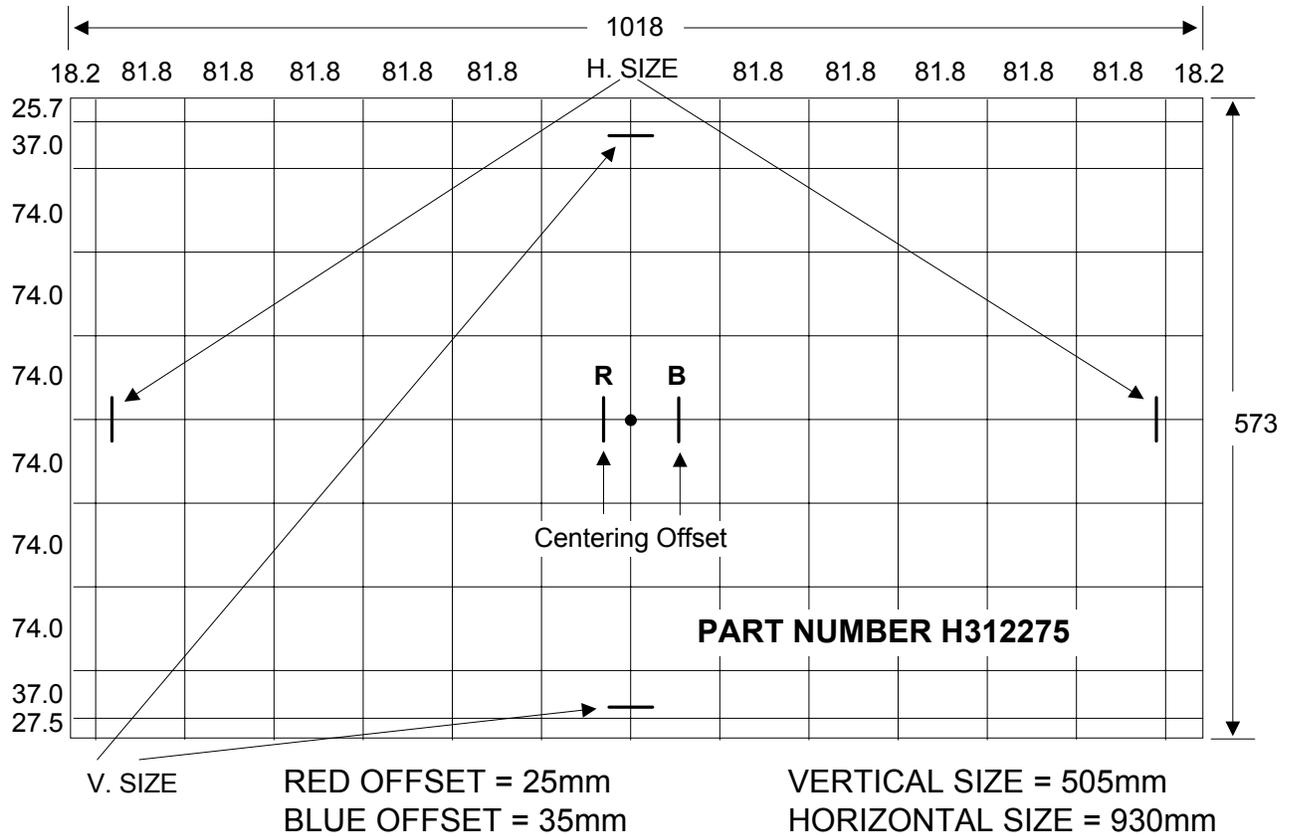


**NOTE: Aspect may not be correct but dimensions are correct.**  
**DIGITAL CONVERGENCE OVERLAY DIMENSIONS**  
**43 inch**  
**OVERLAY DIMENSIONS NORMAL MODE**



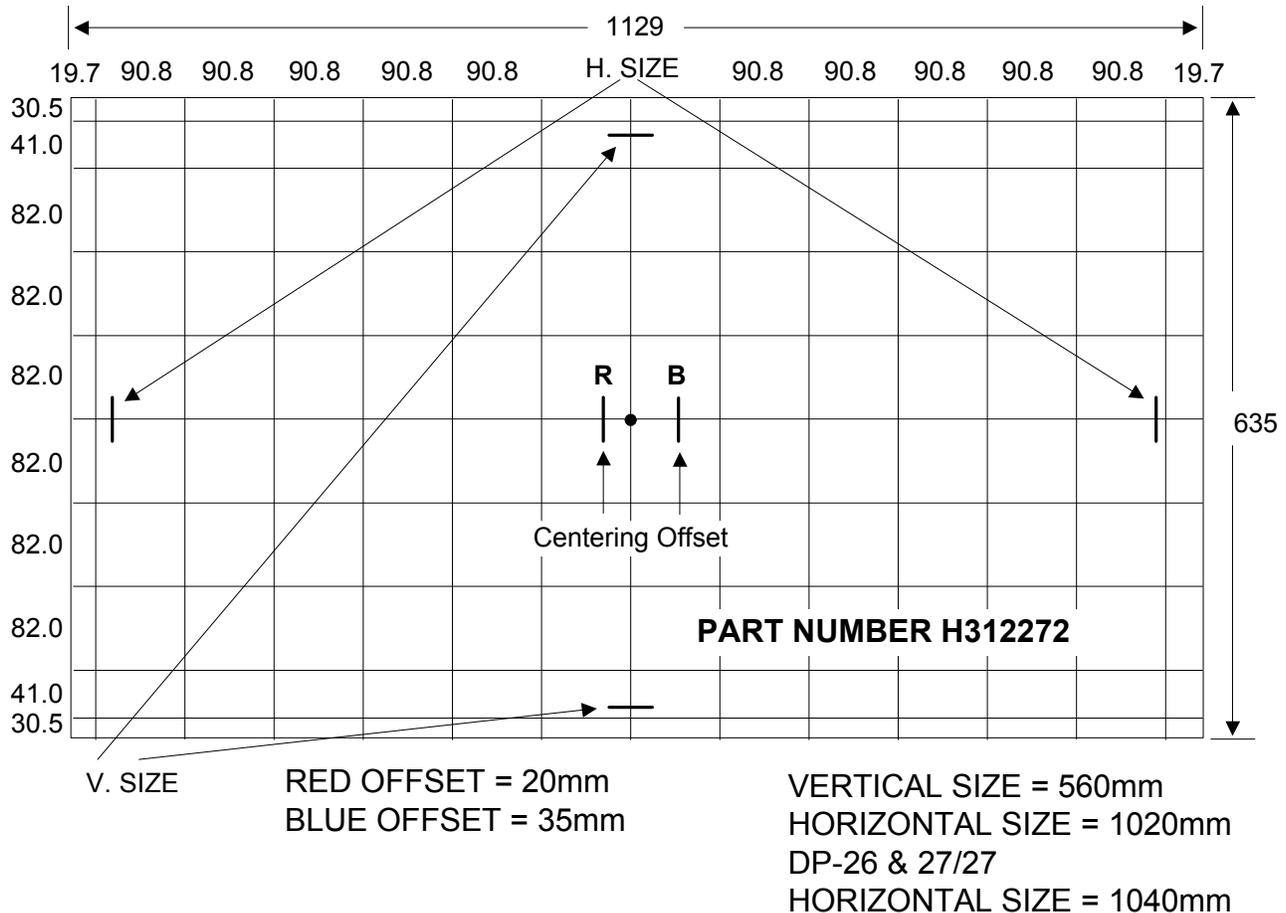
**43FWX20B DP-24 Chassis**

**NOTE: Aspect may not be correct but dimensions are correct.**  
**DIGITAL CONVERGENCE OVERLAY DIMENSIONS**  
**46 inch**  
**OVERLAY DIMENSIONS NORMAL MODE**



**46F500 DP-23K Chassis**

**NOTE: Aspect may not be correct but dimensions are correct.**  
**DIGITAL CONVERGENCE OVERLAY DIMENSIONS**  
**51SWX20B, 51UWX20B, 51GWX20B, 51XWX20B**  
**OVERLAY DIMENSIONS NORMAL MODE**



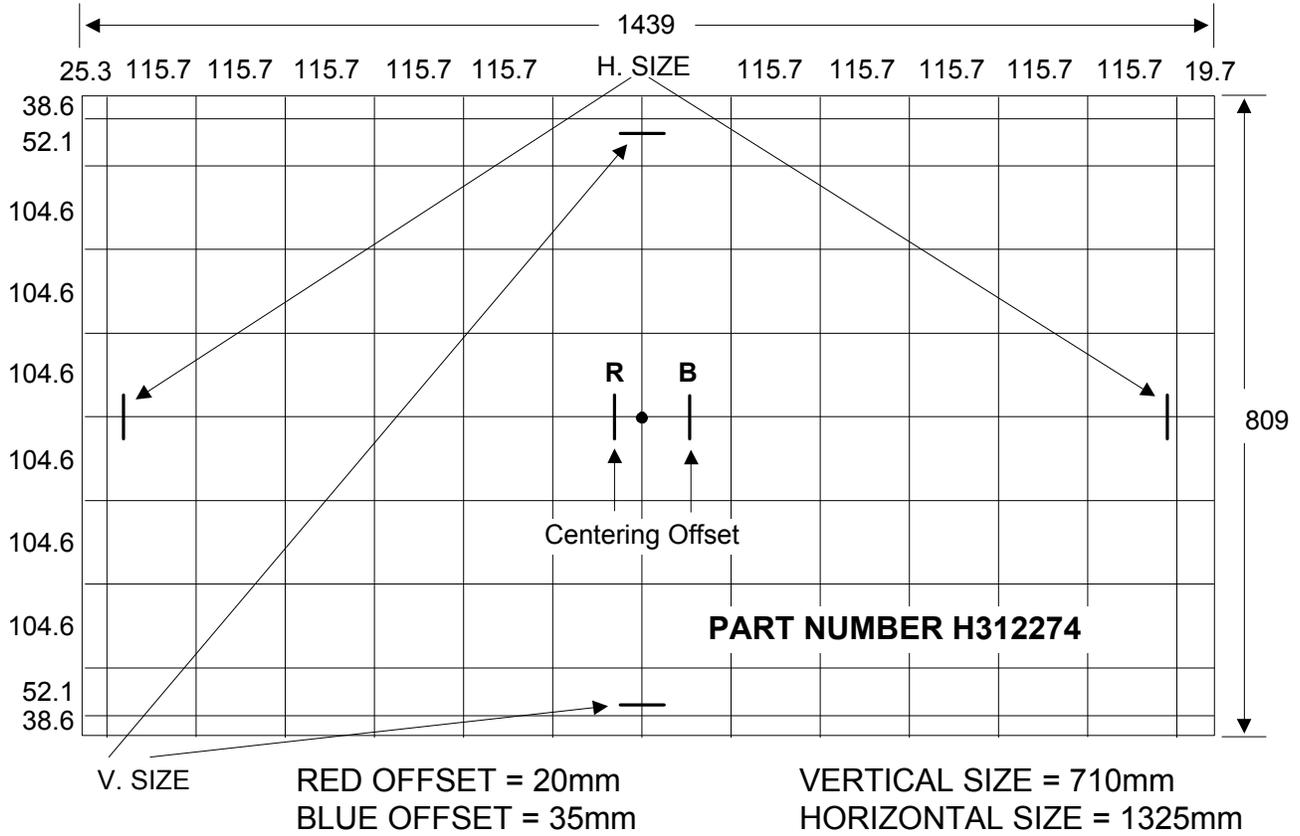
**51UWX20B DP-23 Chassis**  
**51GWX20B DP-23G Chassis**

**NOTE: DO NOT USE THE HORIZONTAL SIZE  
 MARKERS ON THE OVERLAY FOR DP-26 & 27.  
 THESE HAVE BEEN CHANGED. VALUE SHOWN IS CORRECT.**

**51SWX20B DP-27 Chassis**  
**51XWX20B DP-26 Chassis**



**NOTE: Aspect may not be correct but dimensions are correct.  
 65SWX20B, 65TWX20B, 65XWX20B  
 OVERLAY DIMENSIONS NORMAL MODE**



**NOTE: DO NOT USE THE HORIZONTAL SIZE  
 MARKERS ON THE OVERLAY FOR DP-26, 27 & 27D.  
 THESE HAVE BEEN CHANGED. VALUE SHOWN IS CORRECT.**

**65SWX20B DP-27 Chassis  
 65TWX20B DP-27D Chassis  
 65XWX20B DP-26 Chassis**

# **ADJUSTMENT INFORMATION**

**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 7**

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## DP-2X CHASSIS ADJUSTMENT ORDER

It is necessary to follow an order when doing adjustments in the DP-2X chassis.

### DP-2X SERVICE ADJUSTMENT ORDER "PREHEAT BEFORE BEGINNING"

Order	Adjustment Item	Screen Format	Signal	DCU Data
	Pre HEAT (30 Minutes)	Normal Mode	NTSC	N/A
1	Cut Off	Normal Mode	NTSC	N/A
2	DCU Phase Data Setting	Normal Mode	NTSC	N/A
3	Horz. Position Adj. (Coarse)	Normal Mode	NTSC	N/A
4	Raster Tilt	Normal Mode	NTSC	CLEAR
5	Beam Alignment	Normal Mode	NTSC	CLEAR
6	Raster Position	Normal Mode	NTSC	CLEAR
7	Vertical Size Adjust	Normal Mode	NTSC	CLEAR
8	Horz. Size Adjust	Normal Mode	NTSC	CLEAR
9	Beam Form	Normal Mode	NTSC	N/A
10	Lens Focus Adjust	Normal Mode	NTSC	N/A
11	Static Focus Adjust	Normal Mode	NTSC	N/A
12	DCU Character Set Up	Normal Mode	NTSC	N/A
13	DCU Sensor Position	Normal Mode	NTSC	N/A
14	Convergence Alignment	Normal Mode	NTSC	CLEAR
15	Sensor Initialize	Normal Mode	NTSC	N/A
16	Blue Defocus	Normal Mode	NTSC	N/A
17	White Balance Adjustment	Normal Mode	NTSC	N/A
18	Sub Brightness Adjustment	Normal Mode	NTSC	N/A
19	Sub Picture Adjustment	Normal Mode	NTSC	N/A
20	Horz. Position Adjust (Fine)	Normal Mode	NTSC	N/A

Note: To enter the Service I2C Menu;

1. Power should be Off
2. Press and Hold the "INPUT" button on the front control panel.
3. Press the "POWER ON" button while still holding the "INPUT" button.
4. When the power on LED lights, release both buttons.
5. Use the Cursor Up/Down to navigate.
6. Use the Cursor Right/Left button to manipulate the Data Values within the Adjustment.

## DP-2X CHASSIS PRE-HEAT RUN ADJUSTMENTS

**PRESET EACH  
ADJUSTMENT VR TO  
CONDITION AS SHOWN:**

**1. Before Pre Heat Run.**

Enter I<sup>2</sup>C Service Menu.

Pre-set the Green DRV  
and Red DRV to 3F. This  
is considered "Center"  
position.

*(With power Off, press the  
INPUT button on front  
panel and then press the  
POWER ON button then  
release. The Service Menu  
is displayed.)*

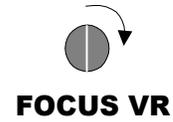
**2. SCREEN VR ON  
FOCUS PACK.**

Pre Set fully counter  
clockwise.

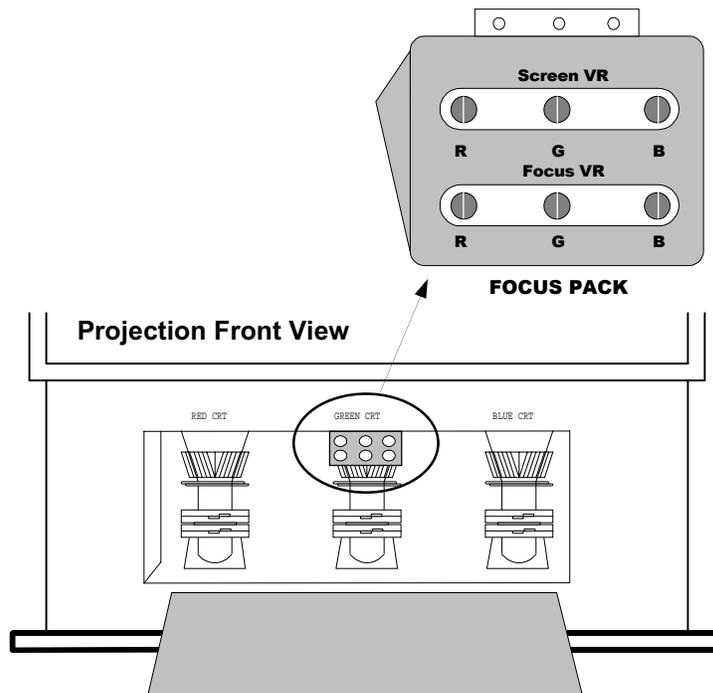
**3. Focus VR on focus pack.**

Pre Set fully clockwise.

**Allow set to operate at  
least 30 Minutes before  
beginning adjustments.**



**SCREEN VR**



## DP-2X CHASSIS CUT-OFF (SCREENS) ADJUSTMENT

### ADJUSTMENT

#### PREPARATION:

- Pre Heat Run should be finished.
- Be sure Screen Color Temperature setting is in the **COOL** mode on Customer's Menu.
- Room Light should be minimal.

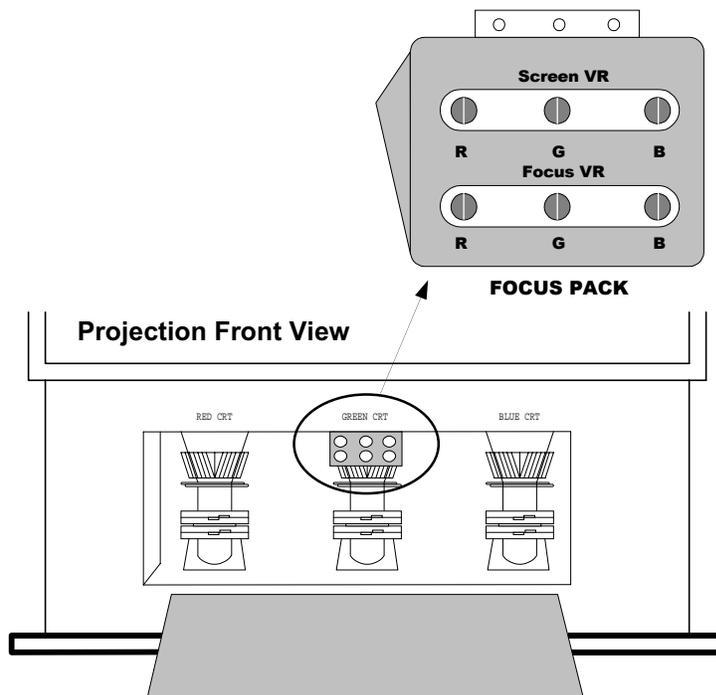
### ADJUSTMENT

#### PROCEDURE:

1) Go to I<sup>2</sup>C ADJ. Mode.

*(With power Off, press the INPUT button on front panel and then press the POWER ON button then release. The Service Menu is displayed.)*

- 2) Set R DRV (COOL) to center data value (**3F**).
- 3) Set G DRV (COOL) to center data value (**3F**).
- 4) Set R, G, and B CUTOFF (COOL) data settings to [**80**].
- 5) Adjust Screen VRs on Focus Pack fully counter clock wise.
- 6) Choose SERVICE item [1] of I<sup>2</sup>C ADJ. Mode. Select CURSOR RIGHT [▶] and the Vertical will collapses.
- 7) Adjust any Screen VR. Screen VR should be turned clockwise gradually until that particular color is barely visible.
- 8) Repeat for the other two colors.
- 9) Exit SERVICE by pressing the cursor on remote to the left [◀].
- 10) Exit SERVICE MENU by pressing the MENU key on remote.



## DP-2X CHASSIS PRE-FOCUS ADJUSTMENT

### ADJUSTMENT

#### PREPARATION:

A) Pre Heat Run should be finished.

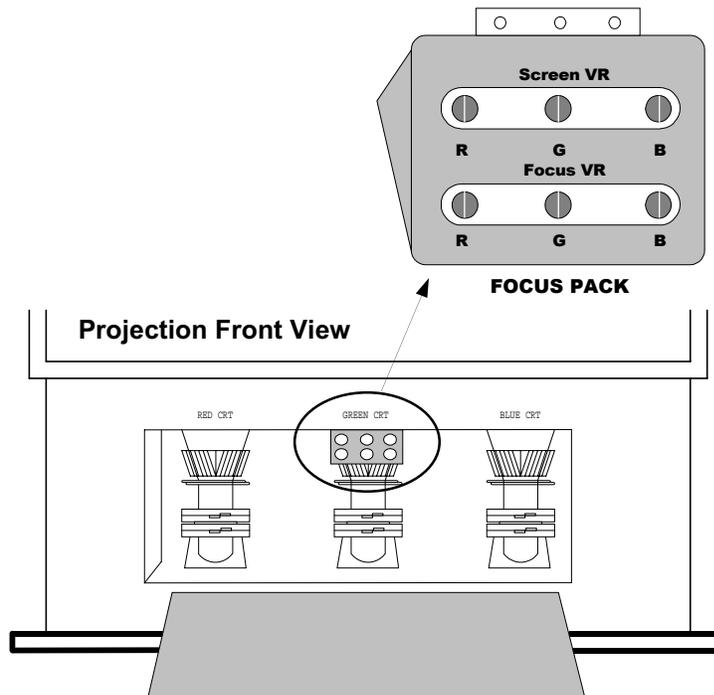
#### FOCUS ADJUSTMENT:

1) Short the 2pin sub-miniature connector on the CRT PWB (PTS), to remove any color not being adjusted and adjust one color at a time. (*The adjustment order of R, G and B is just an example.*)

- 2) Adjust the Focus VR for Red until Focus is achieved. (A Fine Adjustment will be made later.)
- 3) Repeat for Blue and Green.

#### NOTE:

- **PTSR** connector on RED CRT PWB.
- **PTSG** connector on GREEN CRT PWB.
- **PTSB** connector on BLUE CRT PWB.



## DP-2X CHASSIS DCU CROSSHATCH PHASE ADJUSTMENT

### Adjustment Preparation:

- Cut Off adjustment should be finished.
- Video Control: Brightness 90%, Contrast Max.

adjustment mode).

- 6) Adjust data value using the keys indicated in the chart, until the data matches the values indicated in the chart.

**\*DCA** stands for (Digital Convergence Adjustment)

### Adjustment Procedure:

#### **NORMAL MODE**

- 1) Receive any NTSC signal.
- 2) Screen Format is **Normal**
- 3) Press the **SERVICE ONLY** switch on the Deflection/Power PWB to enter DCAM.
- 4) Press the **A/V NET** key on the Remote, Green Cross hatch appears.
- 5) Then press the **EXIT** key. (This is the Phase

#### Exiting Adjustment Mode:

- 7) Press **AV NET** key on remote control.
- 8) Press **PIP MODE** key **TWICE** to store the information.
- 9) When Green dots are displayed, press the **MUTE** key twice to return to DCAM grid.

<b>PHASE MODE</b>	<b>Display Format NORMAL</b>	
<b>ADJUST USING</b>	<b>Address</b>	<b>Data Value</b>
4 and 6 keys on Remote	<b>PH-H</b>	<b>CD</b>
2 and 5 keys on Remote	<b>PH-V</b>	<b>04</b>
Cursor Left and Right on Remote	<b>CR-H</b>	<b>35</b>
Cursor Up and Down on Remote	<b>CR-V</b>	<b>0A</b>

## DP-2X CHASSIS HORIZONTAL PHASE (COARSE) ADJUSTMENT

### **Adjustment Preparation:**

- Video Control: Brightness 90%,
- Contrast Max.

### **Adjustment Procedure**

#### **NORMAL MODE:**

- 1) Receive any NTSC cross-hair signal.
- 2) Screen Format is **NORMAL**.
- 3) Press the **SERVICE ONLY** switch on the convergence PWB and display the Digital Convergence Crosshatch pattern.
- 4) Mark the center of the Digital Convergence Crosshatch Pattern with finger.
- 5) Press the **SERVICE ONLY** switch to return to normal mode.
- 6) Enter the I<sup>2</sup>C Service Menu and select Item **H POSI** and adjust the data so that the center of Video matches the location of the Digital Crosshatch pattern noted in step {4}.
- 7) Exit from the I<sup>2</sup>C Menu.

***NOTE:** To enter the I<sup>2</sup>C Bus alignment menu, with Power Off, press the **INPUT** button and hold it down, then press the **POWER** button and release. I<sup>2</sup>C adjustment menu will appear.*

## DP-2X CHASSIS TILT (RASTER INCLINATION) ADJUSTMENT

### **Adjustment Preparation:**

- The set can face any direction.
- Receive the Cross-Hatch Signal
- **VIDEO CONTROLS:** Factory Preset.
- **SCREEN FORMAT:** should be **NORMAL** mode.
- The lens focus should have been coarse adjusted.
- The electrical focus should have been coarse adjusted.
- The Digital Convergence **RAM** should be cleared. *(Turn power off, press and hold the SERVICE ONLY switch on the Convergence PWB, then press the POWER button).*

### **Adjustment Procedure :**

#### **GREEN:**

- 1) Apply covers to the RED and BLUE lenses or short the 2P Sub Mini connector [PTS] on R&B CRT PWB to produce only **GREEN**.
- 2) Turn the **Green** deflection yoke and adjust the TILT until the green is level.
- 3) [**+/- 2mm tolerance**]. See diagram.

#### **RED:**

- 4) Remove cover or PTS short from **RED** CRT and align RED with GREEN.
- 5) [**+/- 1mm tolerance when compared to Green**]

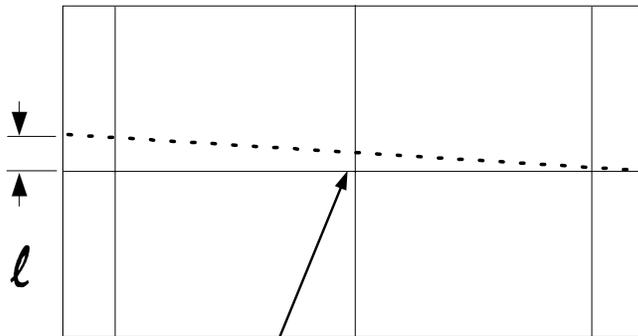
#### **BLUE:**

- 6) Remove cover or PTS short from **BLUE** and cover the RED CRT. Align BLUE with GREEN.
- 7) [**+/- 1mm tolerance when compared to Green**]

#### **After Completion:**

- 8) Tighten DY Yoke Screws to 12+/-2 kg-cm.
- 9) REMOVE ALL COVERS or SHORTS on the PTS connectors.
- 10) Turn the power off.

$$l \leq 2\text{mm}$$



Vertical Center axis of  
Cross-Hair signal

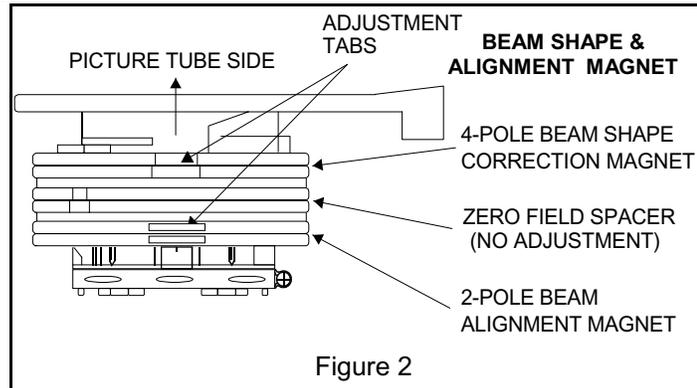
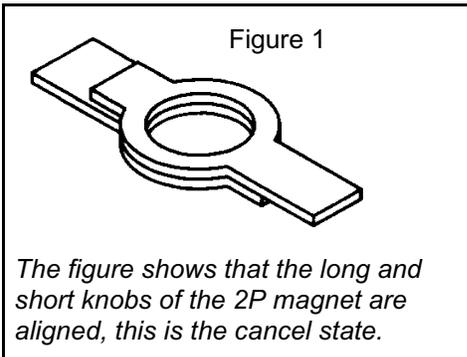
## DP-2X CHASSIS BEAM ALIGNMENT ADJUSTMENT

### Preparation for adjustment:

- Pre Heat, Pre-optical focus, DCU Phase Data, H. POSI Course and Raster Tilt adjustment should be completed.
- Brightness: 90%
- Contrast Max.
- Receive cross hatch signals, or dot pattern
- RASTER TILT adjustment should be finished.
- SCREEN FORMAT should be NORMAL mode.

### Adjustment procedure:

- 1) Green (G) tube beam alignment adjustment:  
Short-circuit 2P subminiature connector plug pins of Red (R) and Blue (B) on the CRT boards and project only Green (G).
- 2) Put Green (G) tube beam alignment magnet to the cancel state as shown in *Figure 1*.
- 3) Turn the Green (G) static focus VR counterclockwise all the way and make sure of position of cross hatch center on screen.
- 4) Turn Green (G) static focus VR clockwise all the way.
- 5) Turn two Beam alignment magnet in any desired direction and move cross hatch center to position found in step (3). (*See Figure 2 below*).
- 6) If image position does not shift when Green static focus VR is turned, adjustment complete.
- 7) If image position does move, repeat steps [2] through [6].
- 8) Conduct beam alignment for Red and Blue in the same way.
- 9) Red (R) focus on focus pack.
- 10) Blue (B) focus on focus pack.
- 11) Upon completion of adjustment, place a small amount of white paint on the beam alignment magnets, to assure they don't move. (*If available*).



**NOTE:** This is the Centering Magnet not the Beam Alignment Magnets. This is just shown for reference, but the principle remains the same.



## DP-2X VERTICAL SIZE ADJUSTMENT

### VERTICAL SIZE:

- 1) Receive an NTSC signal.
- 2) With Power Off, press the Service Only switch on the Convergence PWB. While holding the Service Only Switch down, press the Power On button and Release. DCU Grid will appear without convergence correction. NOTE: After entering DCAM, with each press of the Service Only Switch, the picture will toggle between Video mode and DCU Grid.

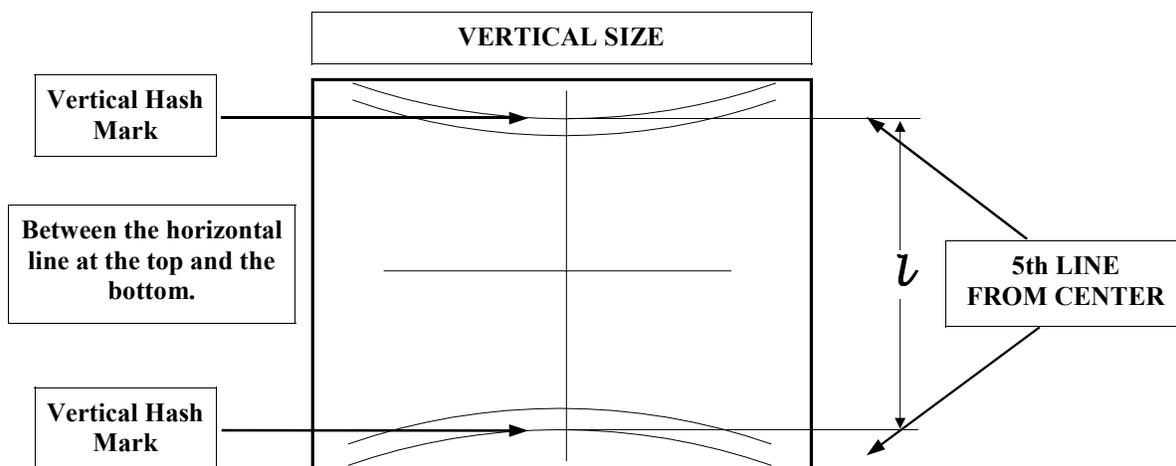
- 3) Select GREEN (A/CH) and press the MENU button to remove Red and Blue.

- 4) **Adjust using R607** (Vertical Size Adj. VR) to match marks on the Overlay. (See Figure Below)

**NOTE: Centering magnet may be moved to facilitate. Distance is important, not centering.**

**NOTE: The Vertical Frequency is shared between Normal and 16X9 HD modes.**

**Alternate Method:**  
Adjust Vertical Size until the size matches the chart below.



DP-2X	$l=$
43 inch	460 mm
46 inch	505 mm
51 inch	560 mm
57 inch	625 mm
65 inch	710 mm

## DP-2X HORIZONTAL SIZE ADJUSTMENT

### HORIZONTAL SIZE: (Display Mode NORMAL)

- Install the correct Overlay.
- Input an NTSC Signal.
- Digital Convergence RAM should be cleared. With Power Off, press the Service Only switch on the Convergence PWB. While holding the Service Only Switch down, press the Power On button and Release. DCU Grid will appear without convergence correction.

NOTE: After entering DCAM, with each press of

the Service Only Switch, the picture will toggle between Video mode and DCU Grid.

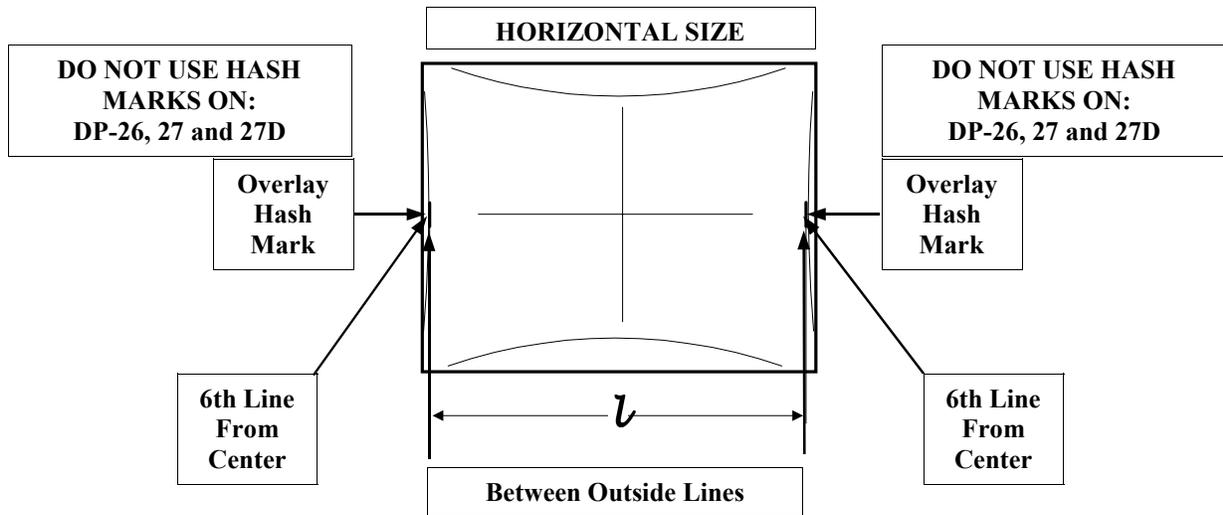
- Project only the Green raster by selecting Green Adjustment mode and pressing the MENU button on remote.

### ADJUSTMENT

1. **Adjust using R711** (Horz. Size Adj. VR) *Adjust Horizontal Size until the size matches the chart below.*
- 2) Press **“Power Off”** to exit

DCAM. (Digital Convergence Adjustment Mode.)

**NOTE: On the DP-26, DP-27 and DP-27D DO NOT USE THE MARKS ON THE OVERLAY. The Horizontal Size adjustment has been increased by 20mm on the 51” and 57” and 25mm on the 61”.**



DP-2X	DP-23/G, 24/K, 25 $l=$	DP-26, DP-27/27D $l=$
43 inch	870 mm	—
46 inch	930 mm	—
51 inch	1020 mm	1040 mm
57 inch	1140 mm	1160 mm
65 inch	1300 mm	1325 mm

## DP-2X BEAM FORM ADJUSTMENT

### BEAM SHAPE (FORM)

#### Preparation for adjustment

- *IMPORTANT: Screen format should be "NORMAL".*
- Pre Heat, Cut-Off, Pre-optical focus, DCU Phase Data, H. Pos Course, Raster Tilt, Beam Alignment, Raster Position, Vertical and Horizontal Size adjustment should be completed.
- Brightness: 90%, Contrast: Max.
- Input a NTSC DOT signal.

#### Adjustments procedure:

- 1) Green CRT beam shape adjustment.
- 2) Short-circuit 2P sub-mini connectors on Red and Blue CRT PWB to project only the Green beam.
- 3) Turn the green static focus VR fully clockwise.
- 4) Make the dot at the screen center a true circle, using the 4-Pole magnet shown in *Figure 2* below.
- 5) Also adjust the Red and Blue CRT beam shapes according to the steps (1) to (4).
- 6) After the adjustment is completed, return R, G and B static VRs to the Best Focus point.

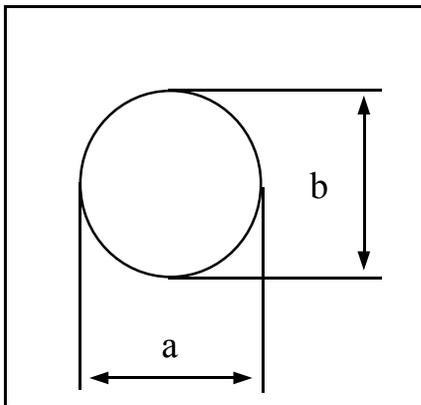


Figure 1

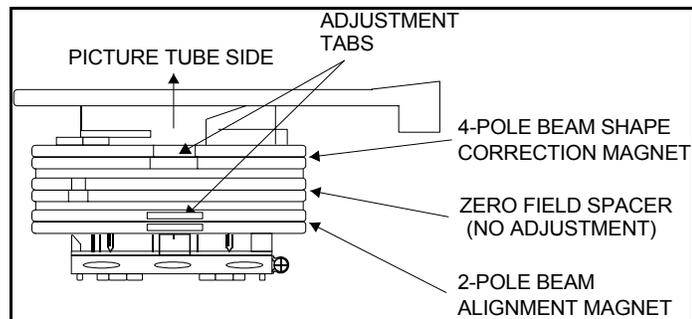


Figure 2

## DP-2X LENS FOCUS ADJUSTMENT

### Preparation for adjustment

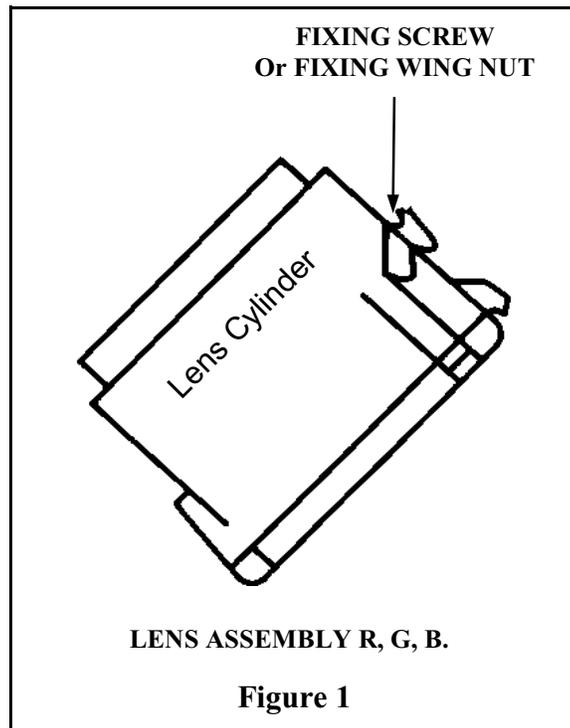
- Receive the Cross-hatch pattern signal.
- The electrical focus adjustment should have been completed.
- Deflection Yoke tilt should have been adjusted.
- Brightness = 50%
- Contrast = 60% to 70%

### Adjustment procedure

- 1) Short the 2 pin sub-miniature connector on the CRT P.W.B. TS, to produce only the color being adjusted and adjust one at a time. (The adjustment order of R, G and B is just an example.)

- 2) (See Figure 1) Loosen the fixing screw on the lens assembly so that the lens cylinder can be turned. (Be careful not to loosen the screw too much, as this may cause movement of the lens cylinder when tightening.)
- 3) Rotate the cylinder back and forth to obtain the best focus point, while observing the Cross-Hatch. (Observe the center of the screen).
- 4) After completing optical focus, tighten the fixing screws for each lens.
- 5) When adjusting the Green Optical focus, be very careful. Green is the most dominant of the color guns and any error will be easily seen.
- 6) Repeat Electrical Focus if necessary.

- *Hint: Located just below the screen are the two wooden panels. Remove the panels to allow access to the focus rings on the Lenses.*



## DP-2X STATIC FOCUS ADJUSTMENT

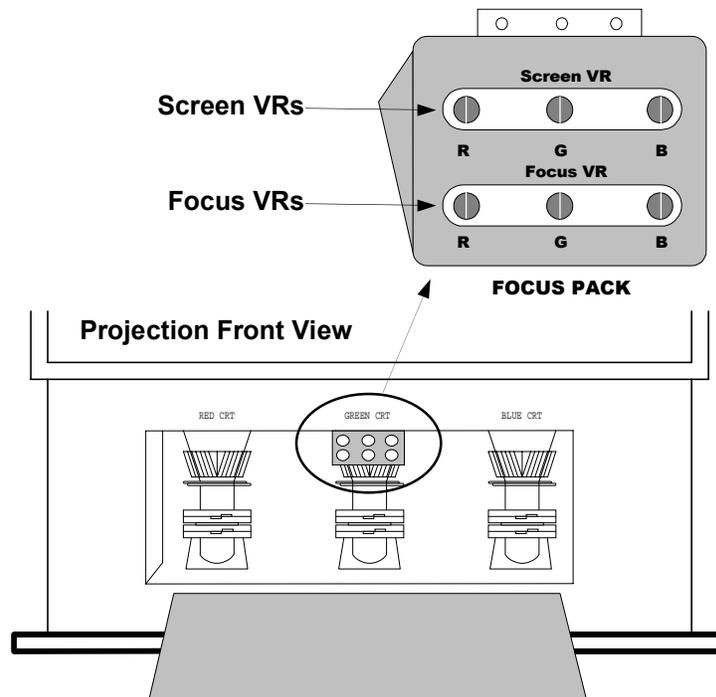
### ADJUSTMENT

### PREPARATION:

- Pre Heat Run should be finished.

### FOCUS ADJUSTMENT:

- 1) Short the 2pin sub-miniature connector on the CRT PWB (PTS), to remove any color not being adjusted and adjust one color at a time. *(The adjustment order of R, G and B is just an example.)*
- 2) Adjust the Focus VR for Red until maximum Focus is achieved.
- 3) Repeat for Blue and Green.



## DP-2X CHASSIS MAGIC FOCUS “CHARACTER SET UP”

**NOTE:** This instruction should be applied when a new DCU is being replaced.

### Adjustment Preparation:

1. Receive NTSC RF or Video Signal.
2. With Power Off, Press and HOLD the **SERVICE ONLY** button on the Convergence/Focus PWB, then press the Power On/Off and release. When picture appears, release Service Only switch. (DCU grid is displayed without convergence correction data.

### Adjustment Procedure:

1. Press the **FREEZE** key on R/C. (One additional line appears near the top and bottom.
2. Press the **PIP CH** key, the ADJ. PARAMETER mode is displayed as following.

### ADJ.PARAMETER

—> **ADJ. DISP. : 77**

**DEMO.WAIT : 2f**  
**INT. START. : 03**  
**V. SQUEEZE :00**

NOTE:

Press the Cursor Left and Right Button to change the ADJ. DISP.

ADJ. DISP Data as follows;

- **77** for **HITACHI**

### **DATA VALUES CONFIRMATION:**

3. Use the Cursor Up and Down keys to scroll through the ADJ. PARAMETER table. Confirm Data values in accordance with **TABLE 1** to the right. To make data value changes, Press the Cursor Left and Right keys.

4. Press the **PIP MODE** key 2 time to write the changed data into EEPROM.
  - First press, ADJ PARAMETER ROM WRITE ? Is displayed for alarm.
  - 2nd press writes data into EEPROM. Green dots appear after completion of operation.
5. Press the **MUTE** button 3 times exit back to DCAM.
6. Press the **Service Only Switch** to exit from DCAM.
7. Power set off.

TABLE 1	DP23 DP23G DP23K Not 46” DP27 / G DP26	DP-23K 46” Only DP24
Parameter	Normal	Normal
ADJ.DISP	77	77
DEMO WAIT	2F	2F
INT. START	03	03
V. SQUEEZE	F0	F0
INT STEP 1	02	02
INT STEP 2	06	06
INT BAR	28	25
INT DELAY	01	01
MGF STEP 1	00	00
MGF STEP 2	06	06
MGF BAR	1B	1B
MGF DELAY	01	01
SEL. STAT.	00	00
LINE WID	1F	1F
ADD LINE	09	09
SENSOR CK	00	00
PORT 0	07	07
PORT 1	06	06
PORT 2	05	05
PORT 3	04	04
PORT 4	03	03
PORT 5	02	02
PORT 6	01	01
PORT 7	00	00
AD LEVEL	03	03
CENT. BAL	00	01
E. DISPLAY	00	00
ADJ. TIMS	60	60
ADJ. LEVEL	05	05
ADJ. NOISE	0A	0A
PHASE MOT	60	60
H. BLK-RV	00	00
H. BLK-GV	01	01
H. BLK-BV	00	00
H. BLK-H	00	00
PON DELAY	0C	0C
IR-CODE	00	00
INITIAL 50	9E	9E
MGF 50	96	96
CENTER 50	FE	FE
STAT 50	FE	FE
DYNA 50	9F	9F

## DP-2X CHASSIS MAGIC FOCUS “PATTERN SET UP”

**NOTE: This instruction should be applied when a new DCU is being replaced.**

**NOTE: This instruction shows how to set up the pattern position for Intellisense. Each model has a specific set up pattern position.**

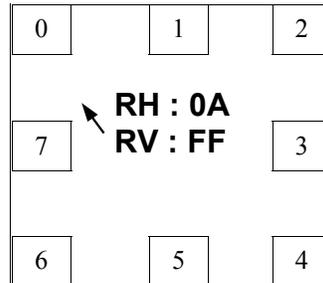
**Adjustment Preparation:**

- Receive NTSC RF or Video Signal.
- With Power Off, Press and HOLD the SERVICE ONLY button on the Convergence/ Focus PWB, then press the Power On/Off at the same time, until picture appears, then release both. (Picture is displayed without conv. Correction data. Press the Service Only button to bring up Internal Crosshatch.)

**Adjustment Procedure:**

1. Press the **FREEZE** key on R/C. (One additional line appears near the top and bottom.

2. Press the;
  - A/V NET key (all but DP-24)
  - **VID2** in (CBL/SAT) (DP-24)
  - The PATTERN mode is displayed as following.



3. Use the 6 Key to rotate Arrow. Arrow rotates clockwise with each press on the 6 Key.
4. Use the following Keys to switch color of patterns.
  - INFO : GREEN
  - 0 : RED
  - ANT : BLUE
5. Press the Cursor Left and Right buttons to change the Pattern Position Data in horizontal Direction. Press the Cursor Up

- and Down buttons to change the Pattern Position Data in Vertical Direction.
6. Set the Data Values as shown in the Table below.
7. Press the **PIP MODE** key 2 times to write the changed data into EEPROM.
  - First press, ADJ PARAMETER ? ROM WRITE ? Is displayed for alarm.
  - 2nd press writes data into EEPROM. Green dots appear after completion of operation.
8. Press the **MUTE** button 3 times exit Pattern Mode.
9. Press the Service Only Switch to exit DCAM.
10. Power set off.

**NORMAL MODE: DP-23, DP-23G, DP-23K Not 46”, DP-26, DP-27 and DP-27G**

	0	1	2	3	4	5	6	7
RH	04	02	FC	FE	FC	02	02	02
RV	03	00	07	01	FB	01	FE	01
GH	04	00	FE	00	FE	00	02	02
GV	04	00	06	01	FC	01	FE	01
BH	06	FE	FC	00	FE	FE	04	02
BV	06	00	04	01	FE	01	FB	01

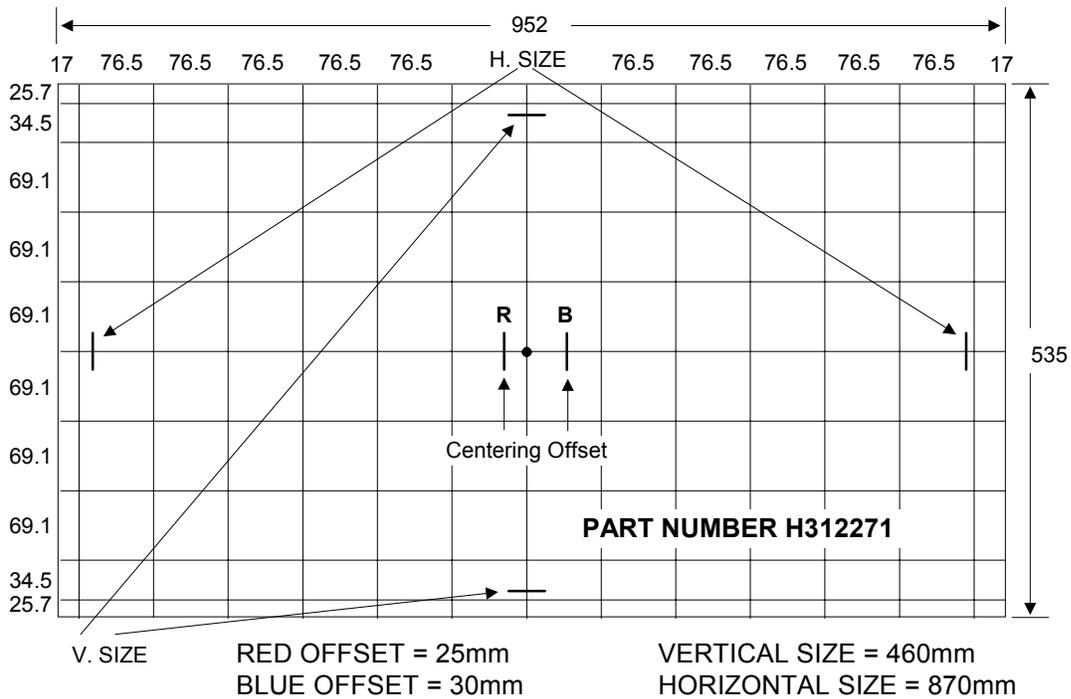
**NORMAL MODE: DP-24 and (DP-23K 46”) DP-23 value in ( )**

	0	1	2	3	4	5	6	7
RH	04	02	FE	00	FE	02	04	02
RV	03	01	06	01	FC	01	FF	01
GH	04	00	FE	00	FE	00	02 (04)	02
GV	04	01	05	01	FD	01	FD	01
BH	04	FC	FE	02	00	FE	04	02
BV	06	01	04	01	FF	01	FD	01

## DP-2X DIGITAL CONVERGENCE OVERLAY DIMENSIONS

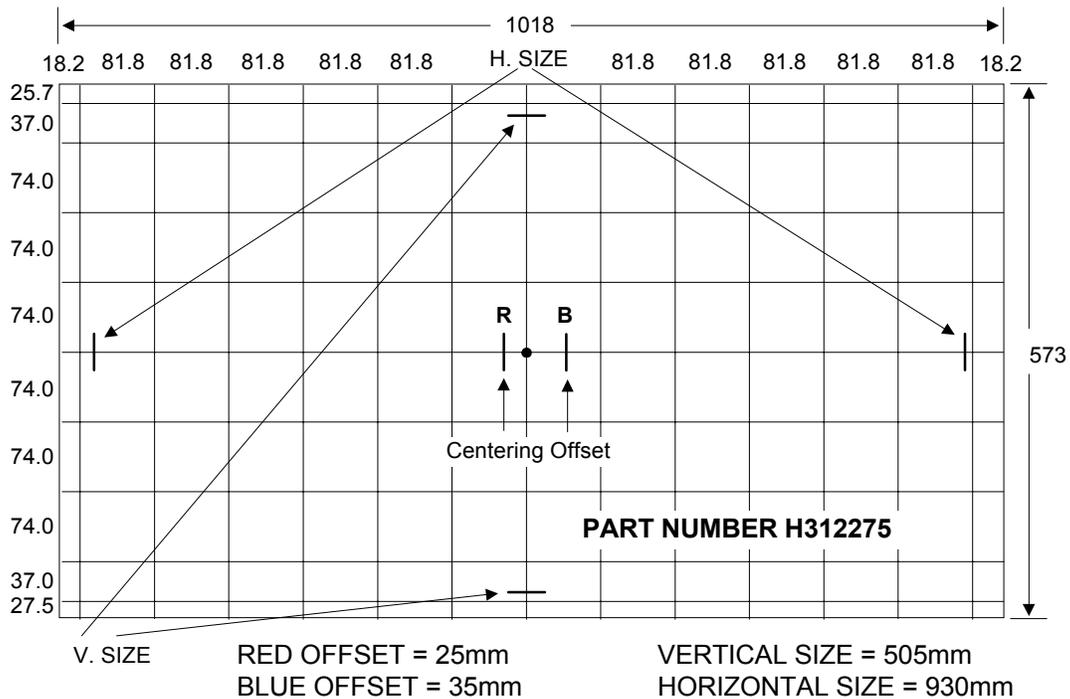
### 43FWX20B DP-23 Only OVERLAY DIMENSIONS NORMAL MODE

*NOTE: Aspect may not be correct but dimensions are correct.*

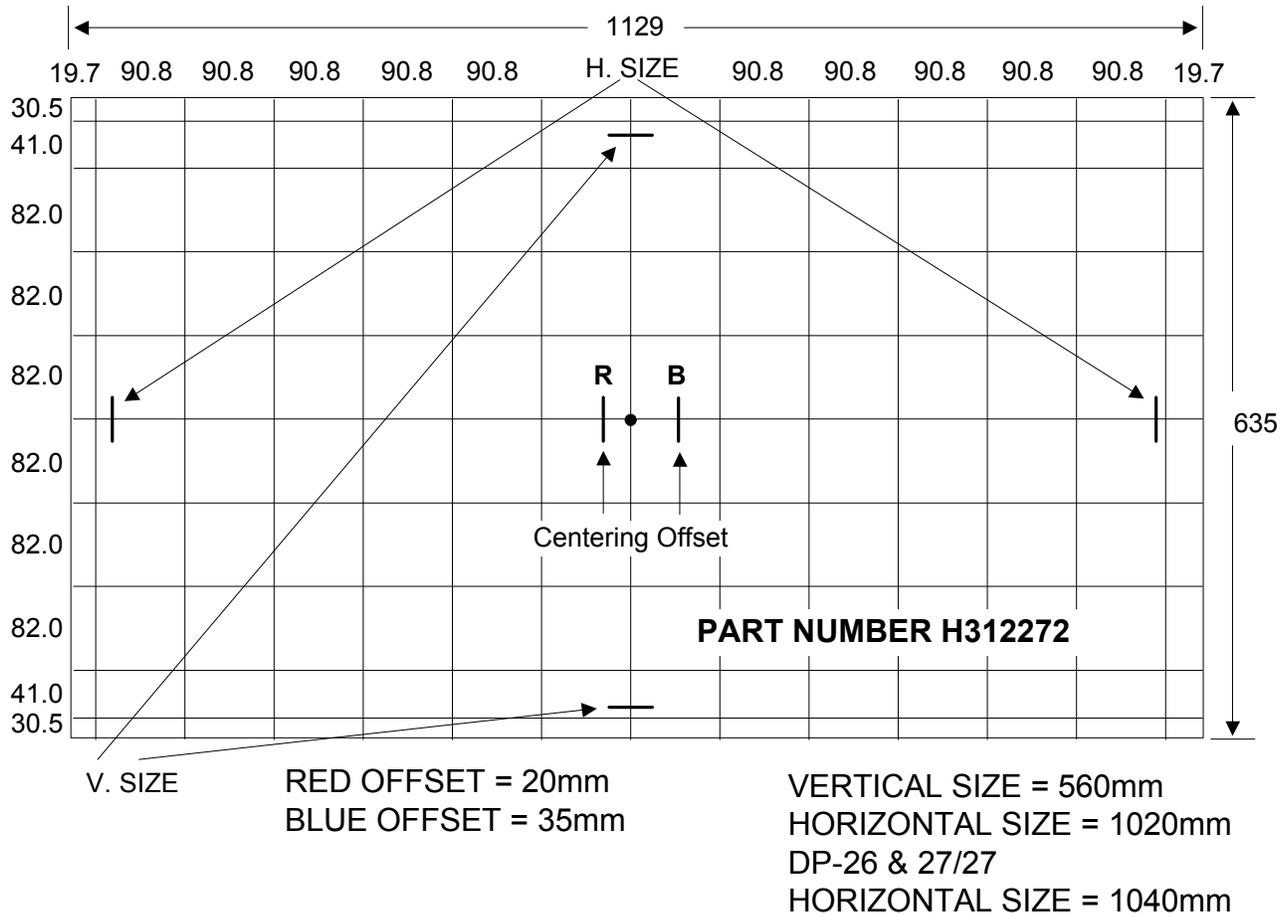


### 46F500 DP-23K Only OVERLAY DIMENSIONS NORMAL MODE

*NOTE: Aspect may not be correct but dimensions are correct.*



**NOTE: Aspect may not be correct but dimensions are correct.**  
**DIGITAL CONVERGENCE OVERLAY DIMENSIONS**  
**51SWX20B, 51UWX20B, 51GWX20B, 51XWX20B**  
**OVERLAY DIMENSIONS NORMAL MODE**



**51UWX20B DP-23 Chassis**  
**51GWX20B DP-23G Chassis**

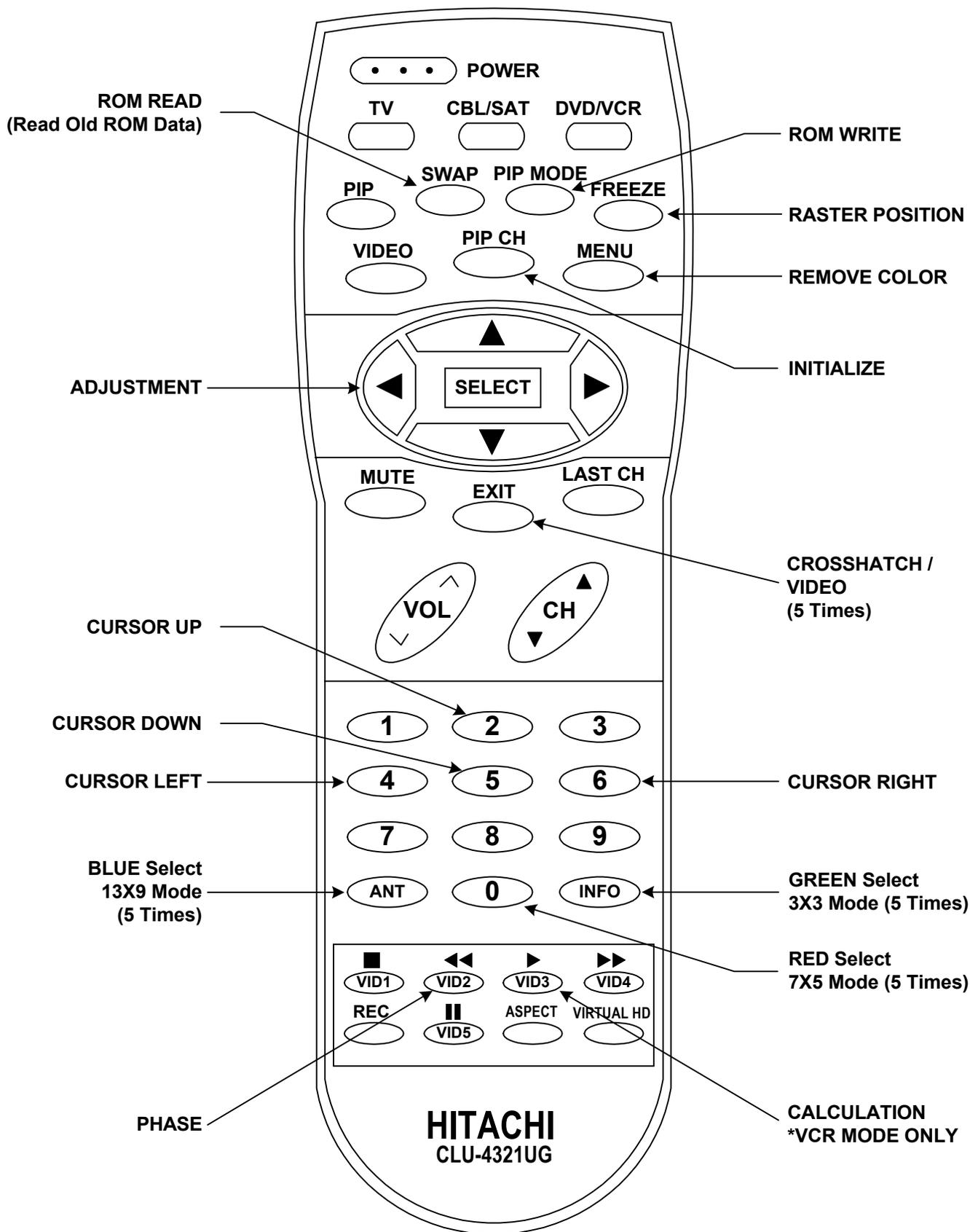
**NOTE: DO NOT USE THE HORIZONTAL SIZE  
 MARKERS ON THE OVERLAY FOR DP-26 & 27.  
 THESE HAVE BEEN CHANGED. VALUE SHOWN IS CORRECT.**

**51SWX20B DP-27 Chassis**  
**51XWX20B DP-26 Chassis**

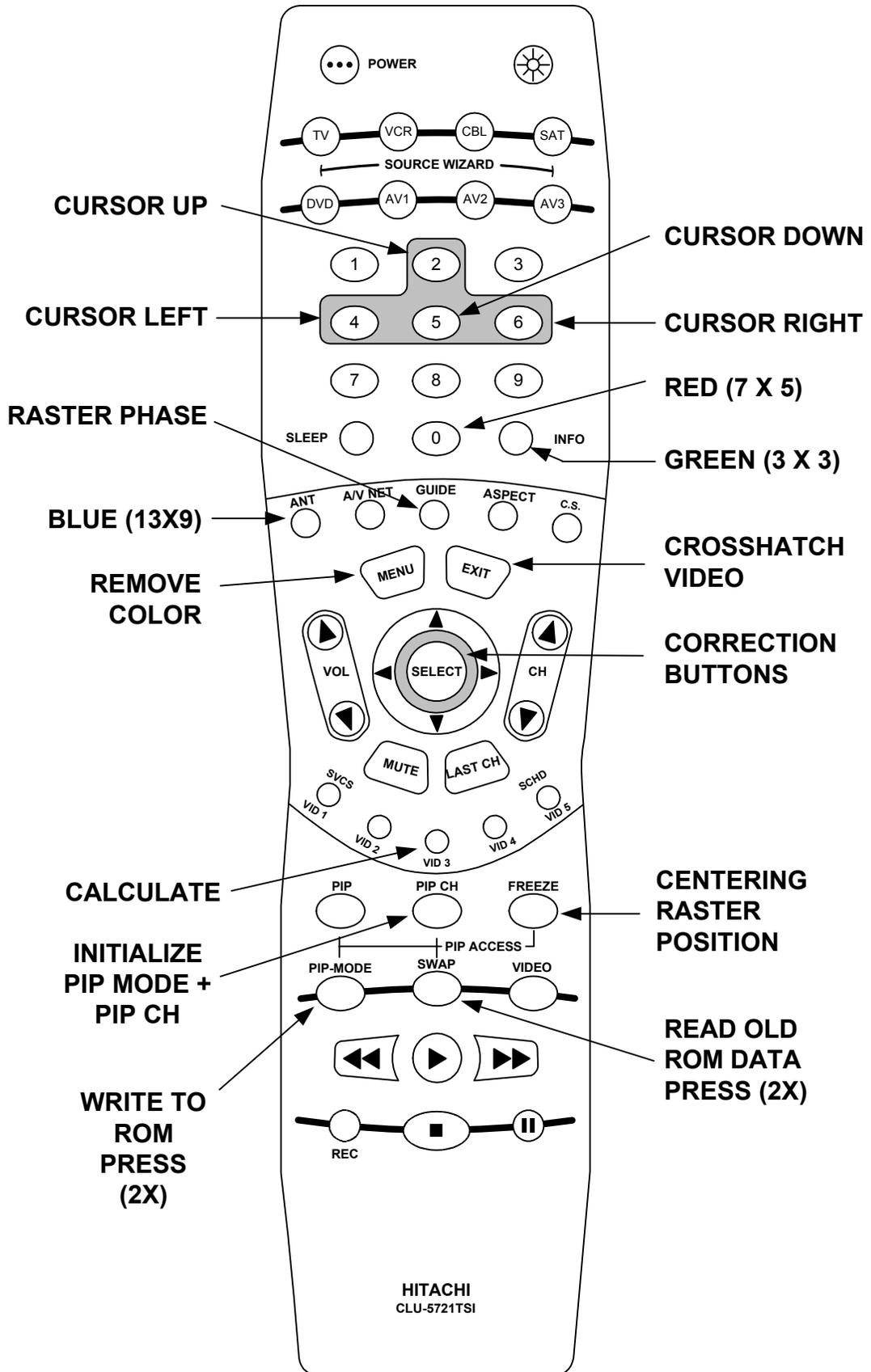




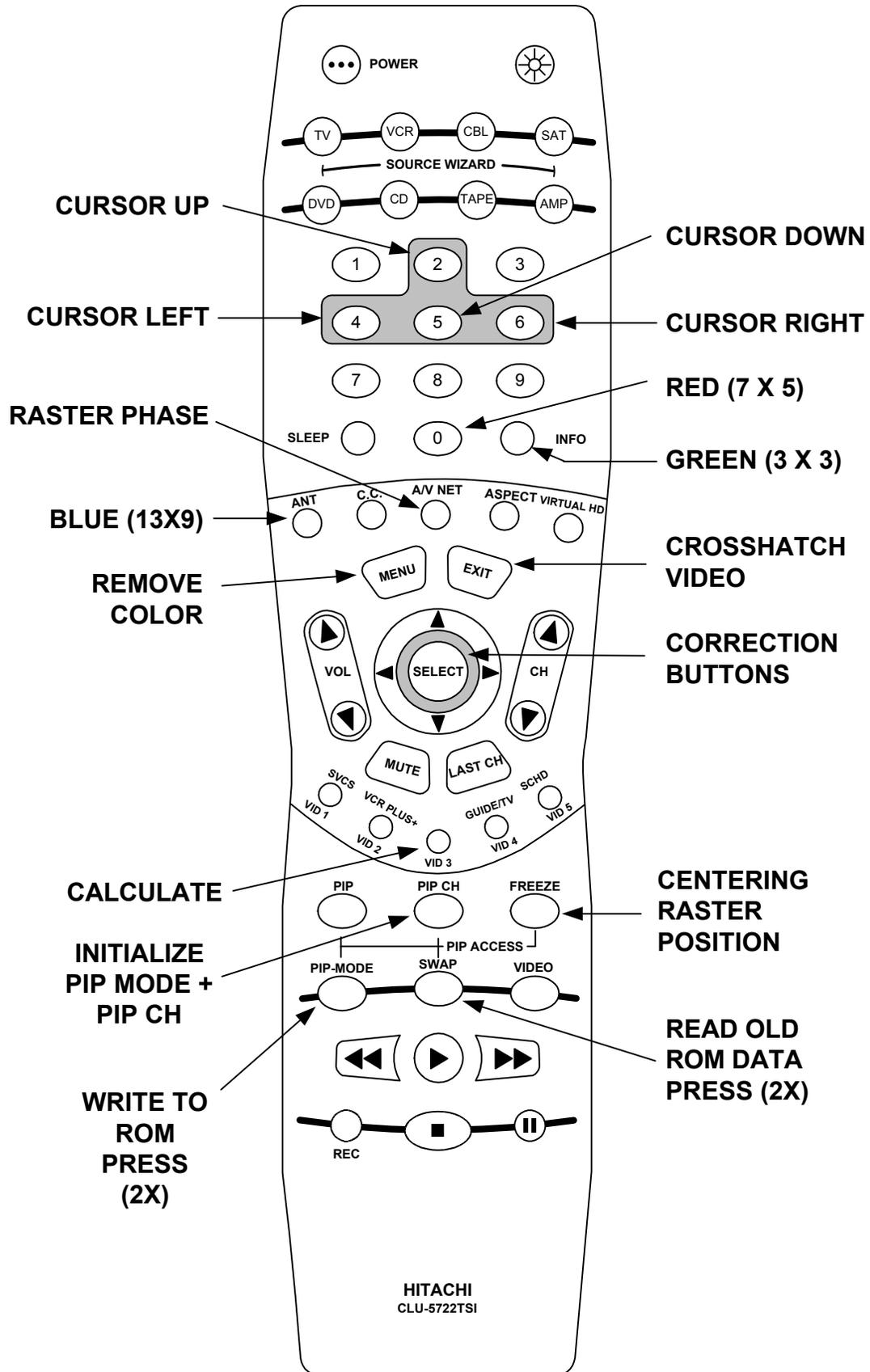
**DP-23, DP-23G & DP-24 REMOTE CONTROL CLU-4321UG (p/n HL01831)  
43FDX20B, 51UWX20B, 57UWX20B, 51GWX20B, 57GWX20B**



**DP-26 REMOTE CONTROL CLU-5721 TSI (P/N HL01821)  
51XWX20B, 57XWX20B, 65XWX20B**



**DP-27 & DP-27D REMOTE CONTROL CLU-5722 TSI (P/N HL01822)  
51SWX20B, 57SWX20B, 65SWX20B, 57TWX20B, 65TWX20B**



## DP-2X CHASSIS READ FROM ROM NOTES

### **BEFORE MAKING ANY DIGITAL CONVERGENCE ADJUSTMENTS**

Heat Run the set for at least 20 minutes.

Do not run Magic Focus before the 20 minutes have passed.

### **MAKE A DETERMINATION:**

- 1) There are many situations where the digital convergence looks as though it may need a convergence adjustment.
- 2) Be sure that it really does before beginning.
- 3) **READ FROM OLD ROM DATA:**
- 4) In any Hitachi Digital convergence set, the Old ROM data can be re-read to place the unit into the last saved condition. This could be beneficial before an attempt to make a rather lengthy adjustment.
- 5) Enter the DCAM.
  - Press the Service Only switch on the Deflection PWB.
- 1) To Read the Old ROM Data, press the **SWAP** button twice.
  - First press: (Read from ROM?) will appear on screen.
  - Second press: Screen goes black, then reappears with green dots.
  - Press the **MUTE** button to return to Digital convergence grid.

### **EXAMPLE:**

Sometimes the Magic Focus will not run correctly and will return an error code.

Sometimes after Magic Focus is run but the convergence appears off after completion.

### **OTHER IMPORTANT INFO:**

Many times after a complete adjustment, when initializing the Magic Focus sensors, an error code will appear, overflow, Error 4, etc...

When this happens, most of the time it is because some critical adjustments were overlooked or skipped.

The below adjustments are very critical to the complete alignment process and **CAN NOT** be overlooked.

- *Vertical Size Adjustment*
- *Horizontal Size Adjustment*
- *Red and Blue Offset Adjustment*
- *DCU Character Adjustment and data confirmation check*
- *DCU Sensor Position Adjustment.*

All of the above adjustment can vary dependent upon the Chassis used. Be sure to check the Service Manual for specifics related to values.

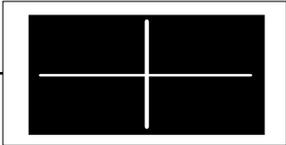
- *In I<sup>2</sup>C Bus adjustment: H. POSI Adjustment*

# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

## Complete Digital Convergence Alignment

Center the Overlay Jig geometrically on the screen

Receive any NTSC signal (Crosshair if possible)  
Set SCREEN FORMAT TO NORMAL mode



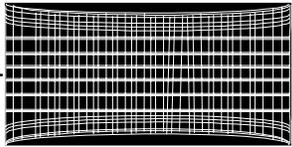
## Clear RAM data (DCU RAM)

Service only switch is on the Deflection PWB.

Press and hold the SERVICE ONLY SWITCH, then press the POWER Button and release, picture appears. Release the SERVICE ONLY SWITCH again. DCU Grid appears.

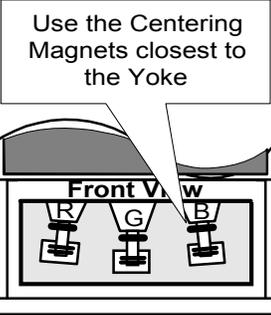
Internal Digital "Cross Hatch Signal" is projected

No DCU Correction added results in severe pincushion distortion



## Center Magnet Adjustments

Select the External Center Cross Signal by pressing the EXIT button 5 times.

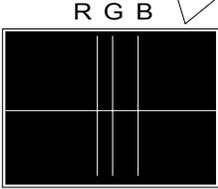


Use the Centering Magnets closest to the Yoke

Align the G,R,B individual center crosses to their respective marks on the Overlay using the Yoke Center Magnets

External Selected Center Cross with no DCU center data

Red = Left  
Blue = Right  
Green = Center



See Offset Chart for exact distances Page 06-09

# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

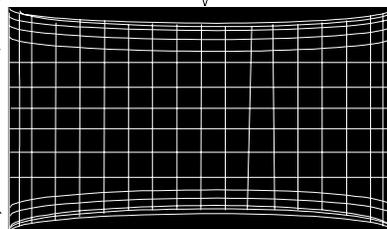
**A**

**Static Centering Alignments (*Moves Entire Raster*)**  
Press EXIT 5 times to return to DCU Grid.

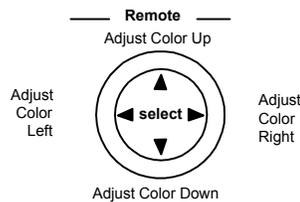
Press the Remote **FREEZE** button (extra lines will appear at top and bottom)

Internal Cross Hatch Signal selected

Extra Lines appear indicating Raster Mode

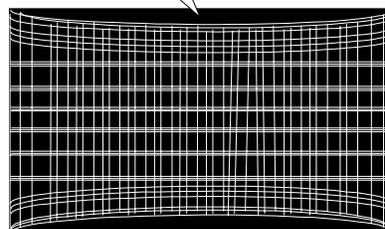


Press the Remote Cursor buttons to match the selected Crosshatch (red and blue) to the green.



**TO SELECT COLORS**  
Info : Selects GREEN  
0 : Selects RED  
ANT : Selects BLUE

Align Red and Blue static centers



Green should already be centered

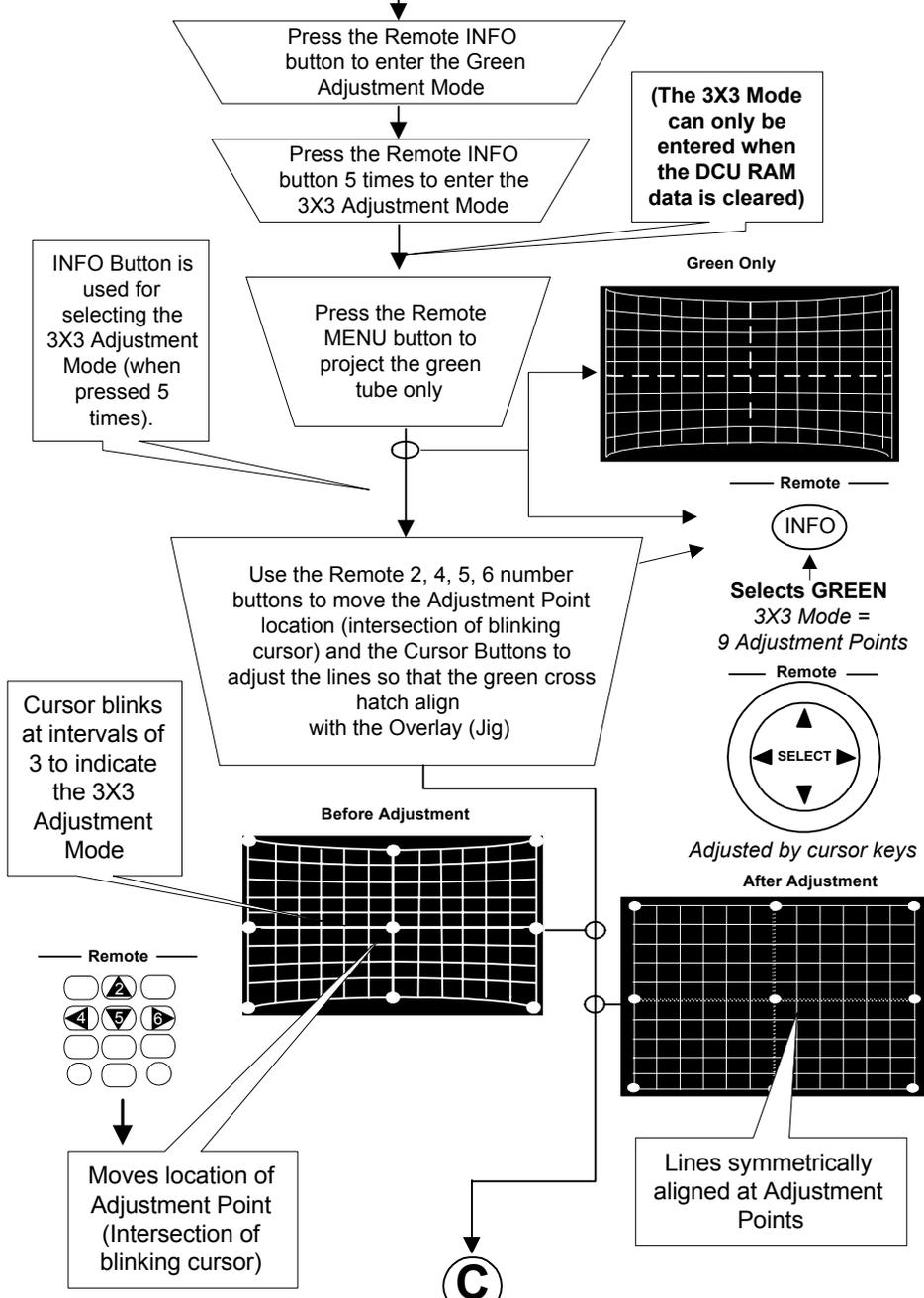
Press the Remote **FREEZE** button to exit Raster Position. (extra lines will disappear)

**B**

# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

**B**

## Convergence 3x3 Point Adjustment Mode (Green Coarse Alignment)



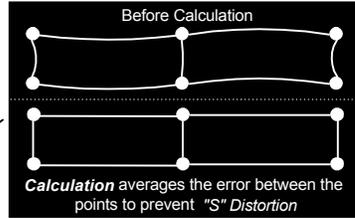
**C**

Continue on next page

# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

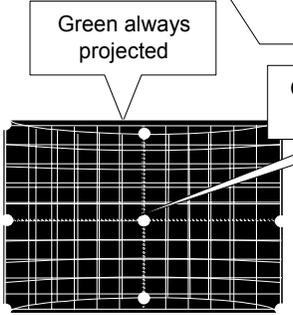
**C**

Press the Remote VID 3 button to Calculate points in between the adjustment points.

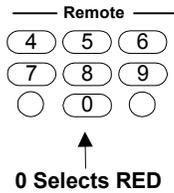


## Convergence 3x3 Mode (9 Point) Adjustment (Red / Blue Coarse Alignment)

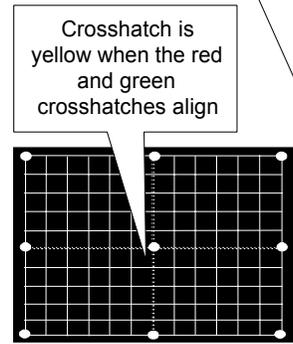
After interpolation, press the Remote0 button to select the Red Convergence Adjustment Mode



Cursor blinks RED

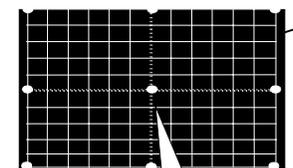
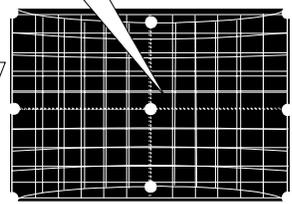


Press the Remote 2,4,5,6 buttons to move the adjustment point, and the Cursor buttons to converge the selected color onto green



Cursor Blinks Blue

Interpolate as often as necessary



Has the Blue 3x3 Convergence Mode been aligned?



Press the Remote ANT button to Select the Blue Convergence Adjustment Mode

Crosshatch is cyan when the blue and green crosshatches align

White internal crosshatch should be projected

Press Menu Button

**D**

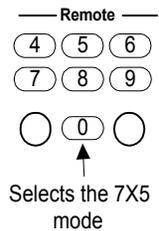
# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

**D**

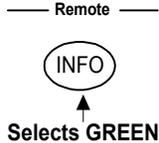
## Convergence 7x5 Point Adjustment (Green Only Alignment)

Press the Remote 0 button five times to enter the 7X5 mode

If selected Color isn't already Red, it will take 6 presses of 0 button

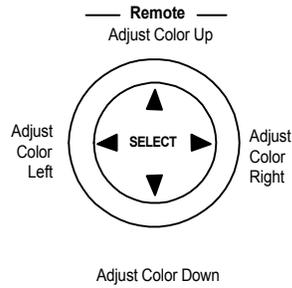
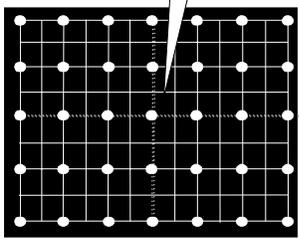


Press the Remote INFO button to project the green only



Use the Remote Cursor and 2,4,5,6 buttons to perform convergence point adjustment at every other intersection of the crosshatch

35 convergence adjustment points in 7X5 mode

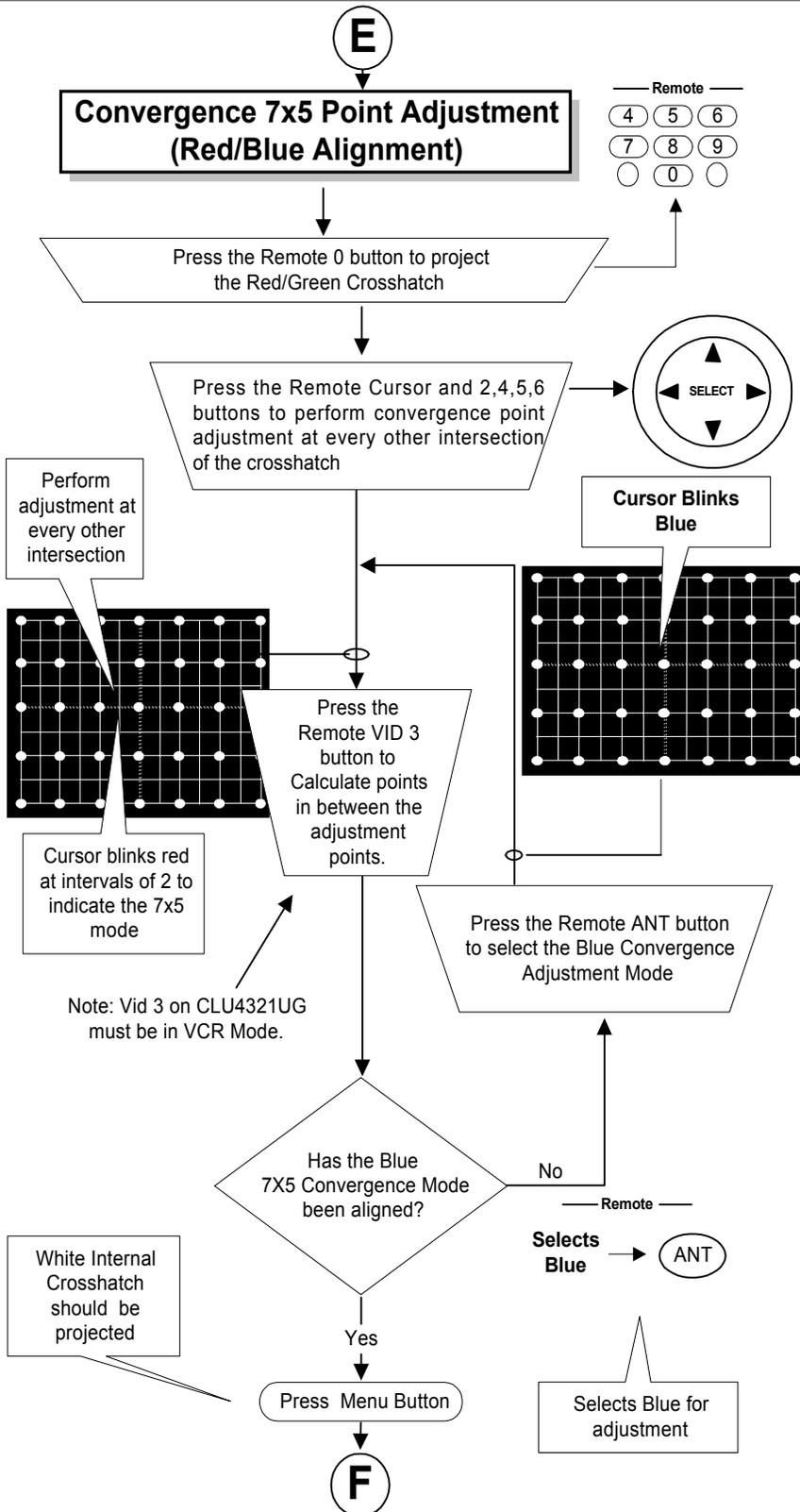


Press the Remote VID 3 button to Calculate points in between the adjustment points.

Note: Vid 3 on CLU4321UG must be in VCR Mode.

**E**

# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES



# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

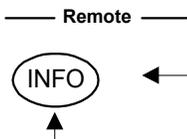
**F**

## Convergence 13X9 Point Adjustment (Green Only Alignment)

Press the Remote ANT  
button five times to  
enter the 13X9 mode

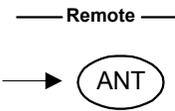
If selected Color isn't already  
Blue, it will take 6 presses  
of Source button

Pressed 5 times,  
Selects the  
13X9 mode

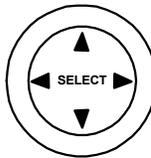


Selects GREEN

Press the Remote A/CH button  
to project  
the green only

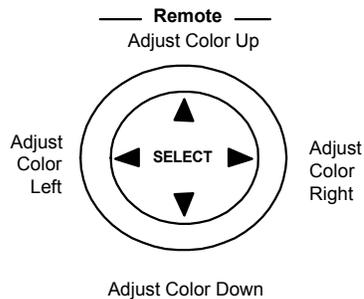
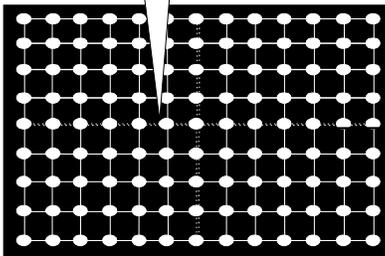


Remote



Use the Remote Cursor and 2,4,5,6  
buttons to perform convergence  
point adjustment at every other  
intersection of the crosshatch

117 convergence  
adjustment points in  
13X9 mode

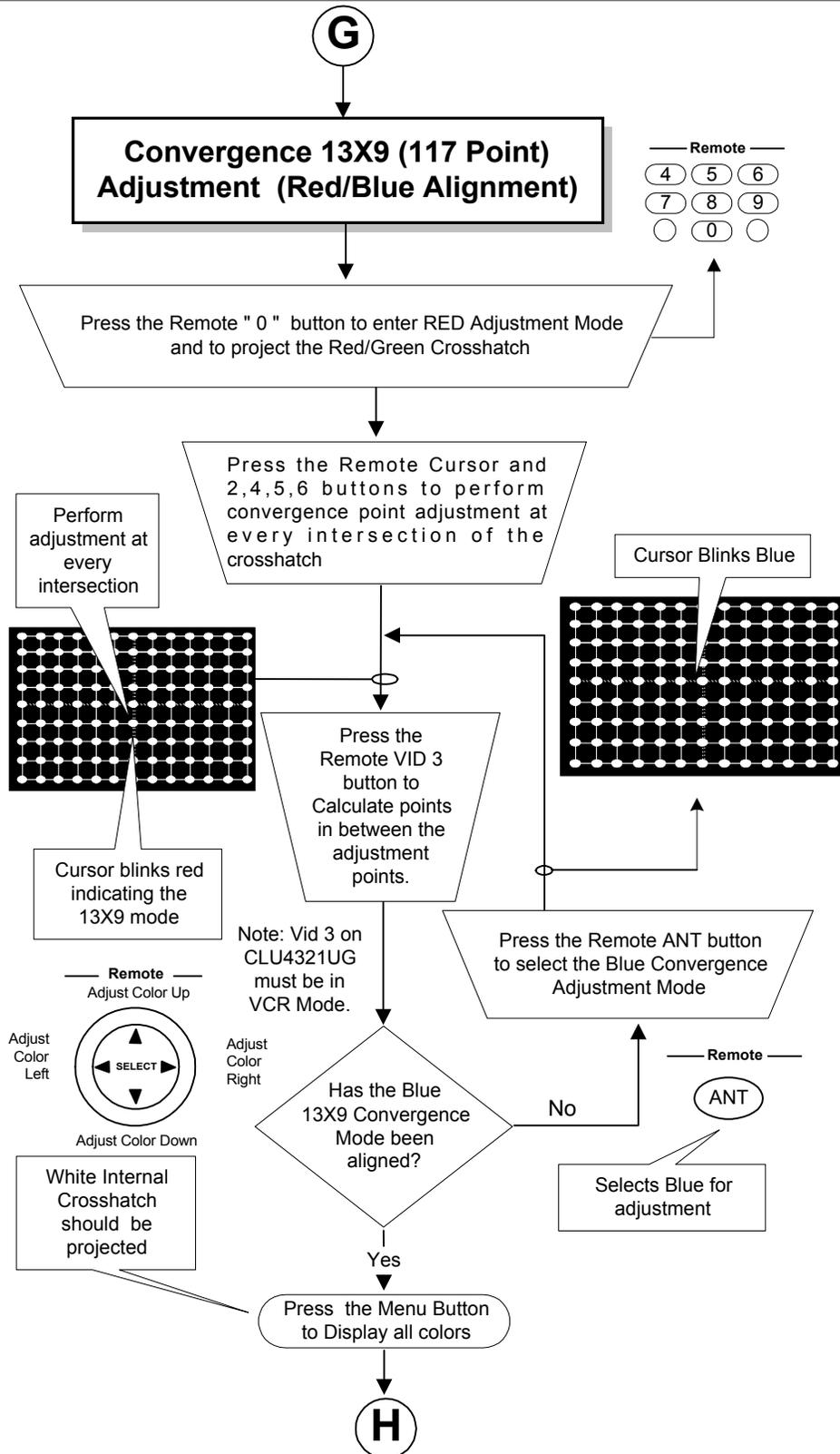


Note: Vid 3 on CLU4321UG  
must be in VCR Mode.

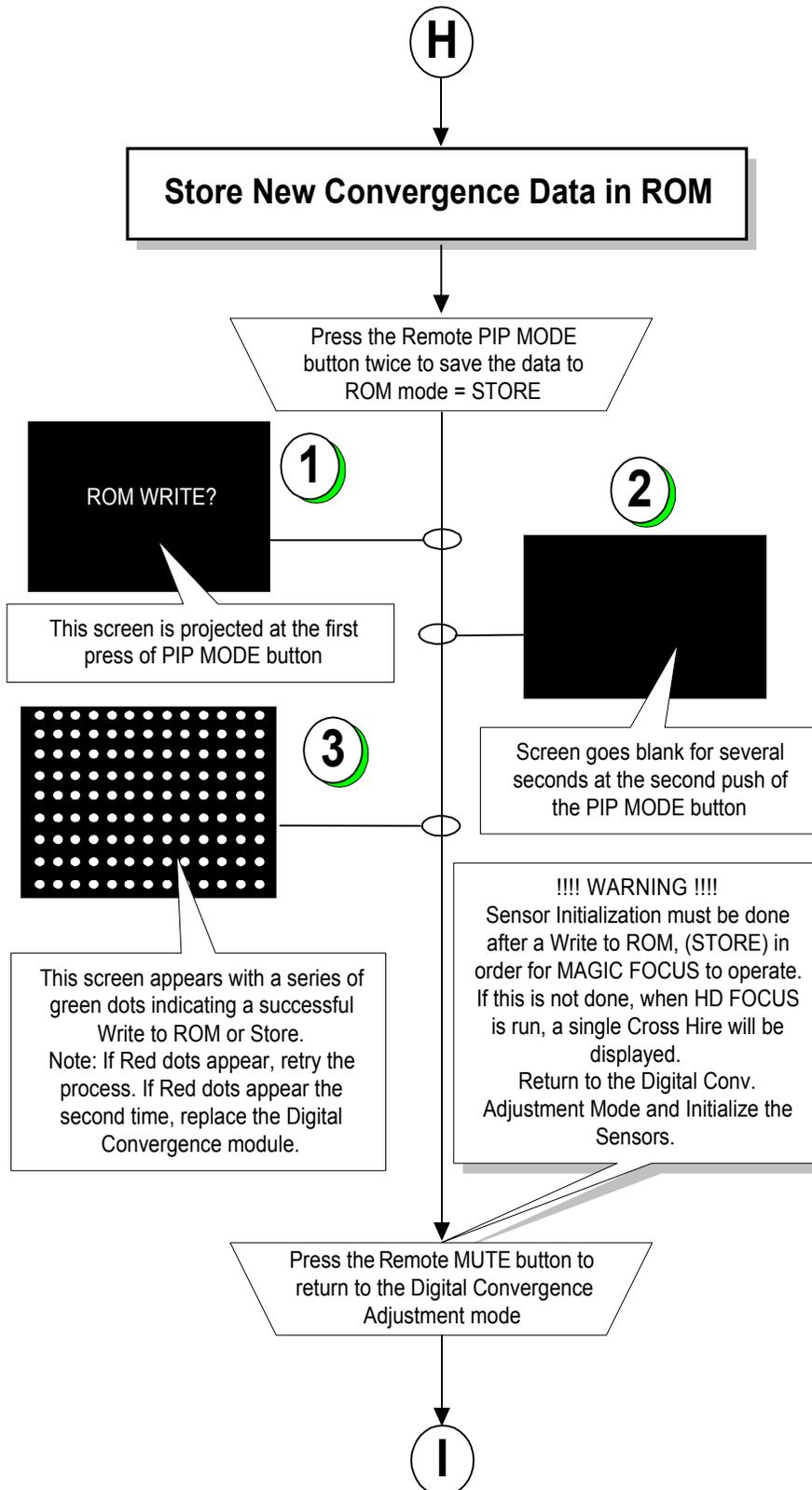
Press the Remote VID 3 button to  
Calculate points in between the  
adjustment points.

**G**

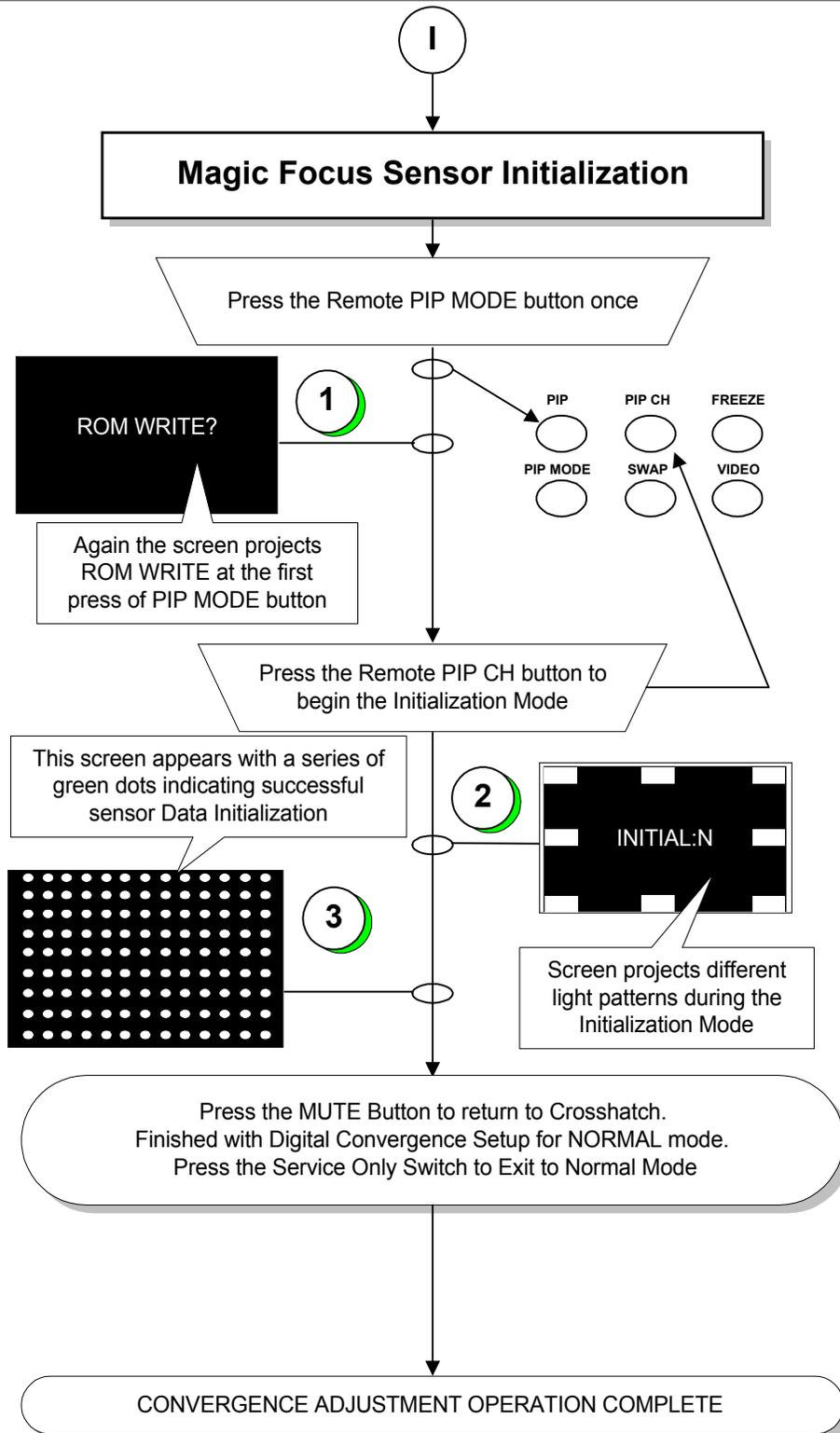
# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES



## DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES



# DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES



## DP-2X DIGITAL CONVERGENCE ALIGNMENT PROCEDURES

### Convergence Touchup Overlays **NOT** required!

Convergence Point Adjustment.  
NTSC (Normal).

Enter the Service Mode by pressing the Service Only Switch on Power/Deflection PWB.

Press "0" five times to select the 7X5 Mode  
Press "ANT" five times to select the 13X9 Mode  
Note: 3X3 mode can not be entered without clearing RAM data.

Cleared RAM data mode can be entered if necessary.  
Clear RAM data by pressing and holding the Service Only button, then press the Power button. Press the Service Only switch again to display the DCU Grid, then Read the Old ROM data. (SWAP pressed twice)

Press the MENU button to Remove colors not being adjusted.

Press 2, 4, 5, 6 buttons to move Adjustment Point  
Press Cursor Up / Down / Left / Right to Adjust Convergence

When adjustment is complete, STORE the New DATA by pressing the PIP MODE button twice.  
Press the MUTE button to return to DCAM grid.

After Storing, initialize the sensors by pressing the PIP MODE button ONCE and then press the PIP CH button.  
Press the MUTE button to return to DCAM grid.  
See "Complete Digital Convergence Alignment procedure" for more details.

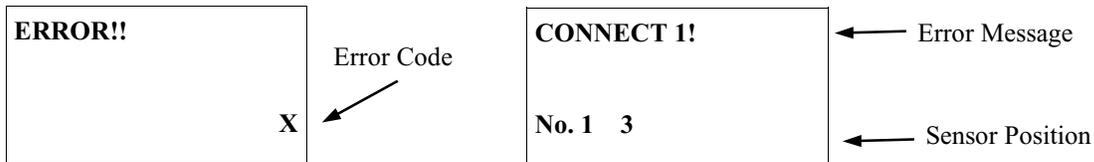
Press the Service Only Switch  
to Exit DCAM mode.

## MAGIC FOCUS ERROR CODES FOR THE DP-2X CHASSIS

### CONVERGENCE ERRORS:

If an error message or code appears while performing MAGIC FOCUS or initialize (PIP MODE and PIP CH in Digital Convergence Adjustment Mode, follow this confirmation and repair method.

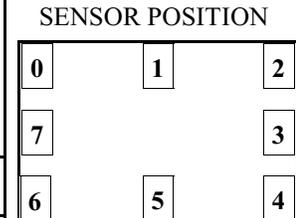
- 1) Turn on Power and receive any signal.
- 2) Press the Service Only Switch on the Convergence Output PWB.
- 3) Press **SWAP** and then the **PIP CH** buttons on the remote control.
- 4) Error code will be displayed in bottom right corner of screen.
- 5) If there is no error, and **INITIAL OK** will appear on screen.



6) Follow repair table for errors.

### ERROR!!.

Error Code	Error Display Code	Countermeasure	Application	
			Initialize	Magic Focus
1	VF Error	Replace DCU	X	X
2 *2	Connect 1	1. Darken Outside Light 2. Placing of Sensor 3. Is pattern hitting sensor? 4. Check connection and solder bridge of sensor 5. Replace Sensor. 6. Replace Sensor PWB. 7. Sensor Connector check. 8. Replace DCU. 9. Adjustment check (H/V size, centering).	X	—
3*2	A/D Level	Same as Error Code 2	X	X
4	Over Flow	1. Check the placement 2. Adjustment check (H/V size, centering). 3. Conv. Amp. Gain check*1 (check resistor values only)	X	X
5	Convergence	Same as Error Code 4	X	X
7	Operation	Same as Error Code 4	—	X
9	Connect 2	Same as Error Code 2	X	X
10	Noise	Input strong field. Strong signal. Check the wiring of connector between sensor and DCU	X	X
11	Sync	Input strong field. Strong signal. Check the wiring of connector between sensor and DCU	X	X



\*1 = RK 42, 46, 50, 54, 58, 62 check these resistors. \*2 = Sensor Position

## DP-2X BLUE DE-FOCUS ADJUSTMENT

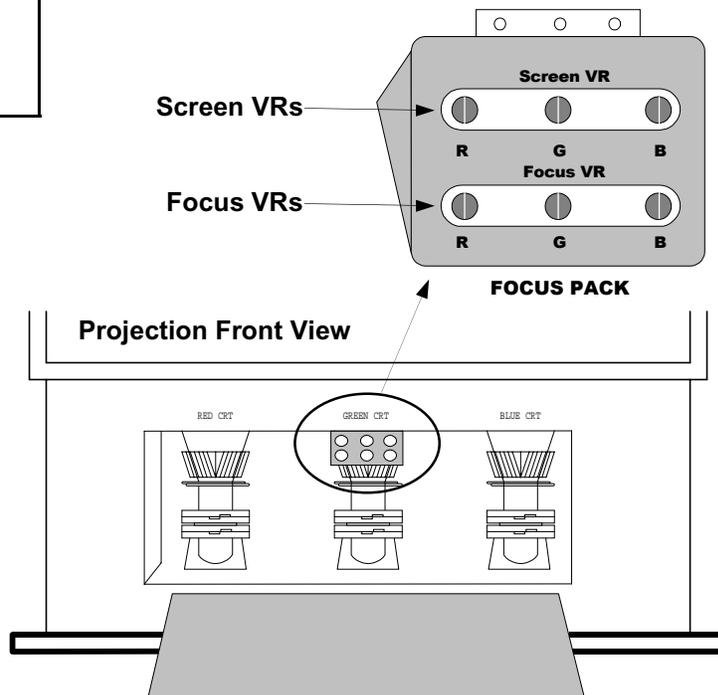
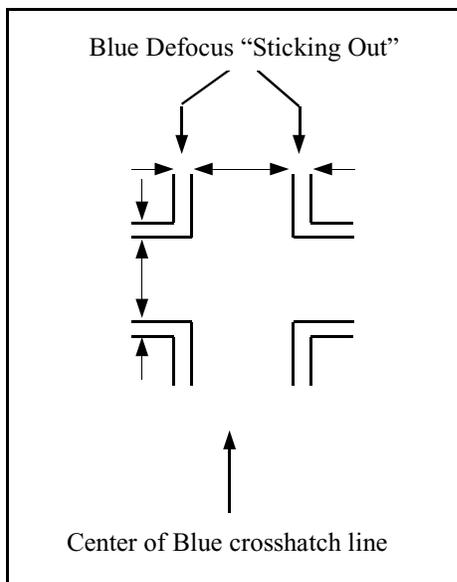
### Adjustment Preparation:

- Video Control: Brightness 90%, Contrast Max.
- SCREEN FORMAT should be PROGRESSIVE mode.

### Adjustment Procedure

- 1) Receive any NTSC cross-hatch signal.
- 2) Turn the **B FOCUS VR** fully clockwise.
- 3) Adjust BLUE defocus according to the following specifications.

*1mm on each side equaling 2mm total. See figure Below.*



## DP-2X WHITE BALANCE and SUB BRIGHTNESS ADJUSTMENT

### Adjustment Conditions:

- Cut Off and Blue Defocus must be complete.
- High brightness white balance
- Low brightness white balance

### Screen adjustment VRs on Focus Block

### Drive adjustment performed using I<sup>2</sup>C Bus Alignment within Service Menu.

### Preparation for adjustment

- Start adjustment 20 minutes or more after the power is turned on.
- Turn the brightness and black level OSD to minimum by remote control.
- Receive a tuner signal, (any channel, B/W would be best).
- Set the Green and Blue drive adjustment within I<sup>2</sup>C Service Menu to their Data Centers (3F).
- R, G, and B Cutoff should be set to (7F).
- Set Color Temperature to COOL on Customer's Menu.

### Adjustment procedure

#### Sub Brightness:

- 1) Go to I<sup>2</sup>C ADJ. Mode. With power Off, press **INPUT** and **POWER** buttons at the same time, then release. Service Menu is displayed.
- 2) Adjust the Sub Brightness Number [2] SUBBRT using I<sup>2</sup>C Bus alignment procedure so only the slightest white portions of the raster can be seen.
- 3) Exit Service Menu by pressing **MENU** button.
- 4) Input a gray scale signal into any Video input and select

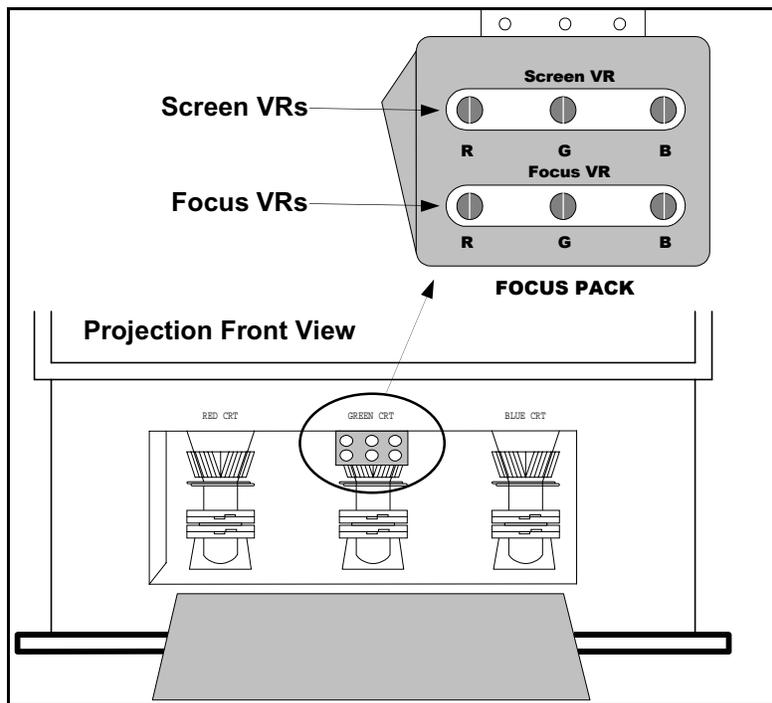
that input using the VID buttons on the remote or front control panel.

- 5) Turn the Brightness and Contrast OSD all the way up.
- 6) Enter the Service Menu again.
- 7) Make the whites as white as possible using the Red DRV (Cool) and Green DRV (Cool) Drive adjustment within I<sup>2</sup>C Service Menu . (10800K). X=0.278 Y=0.280.
- 8) Set the Brightness and Contrast to minimum.
- 9) Adjust the low brightness areas to black and white, using screen adjustment VRs (red, green, blue) on the Focus Block assembly. (10800 K)
- 10) Check the high brightness whites again. If not OK, repeat steps 6 through 9.
- 11) Press the **MENU** key on

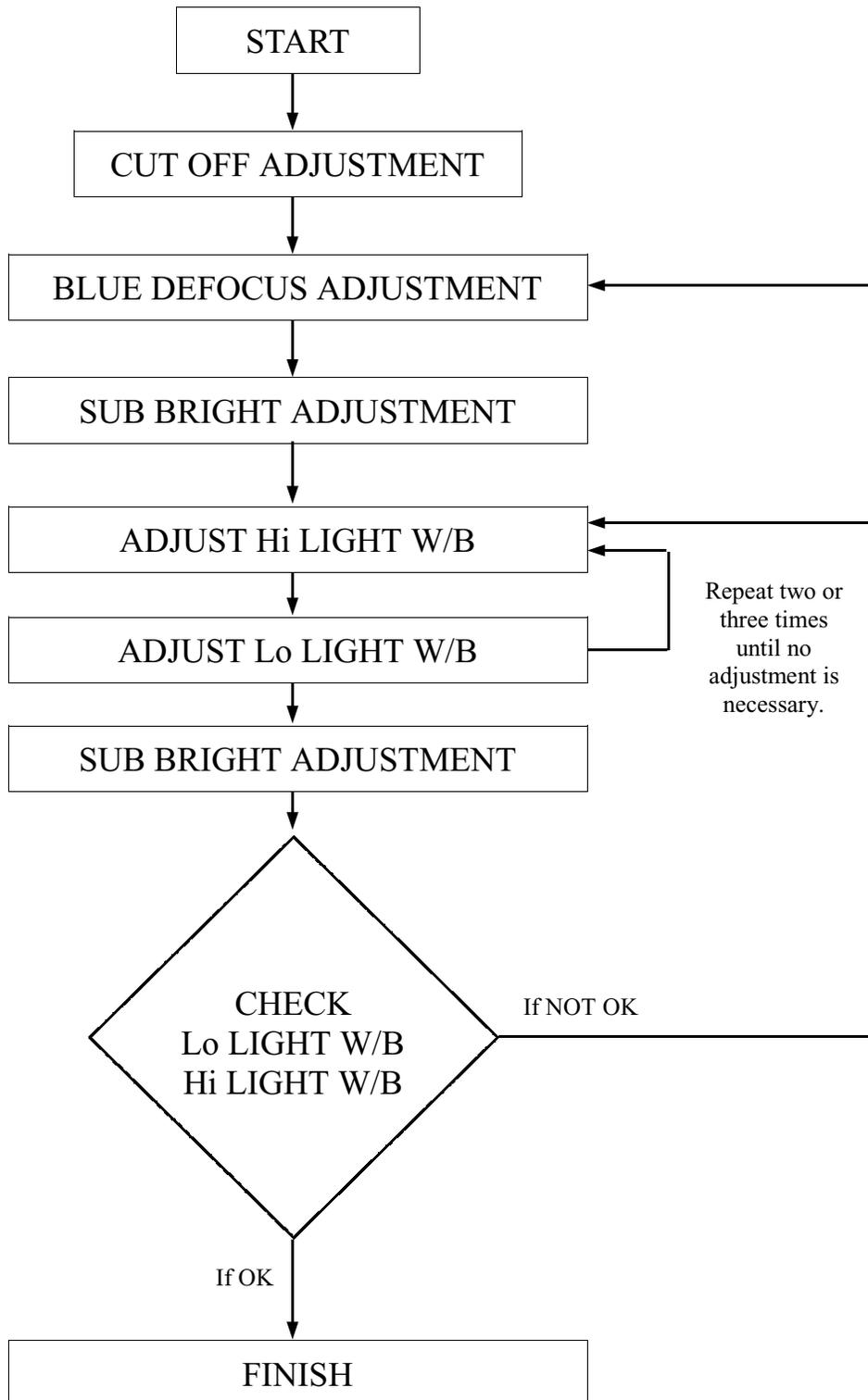
remote to Exit Service Menu.

Remember: When adjusting the Screen controls. After the Cut Off adjustment has been completed, never adjust the controls clockwise. Always adjust counter clockwise. This lengthens tube life.

Also, do not use the Focus Block adjustments, use I<sup>2</sup>C R, G and B Cutoff adjustments. Green is reference, do not adjust.



# DP-2X WHITE BALANCE ADJUSTMENT FLOW CHART



## DP-2X SUB PICTURE AMPLITUDE ADJUSTMENT

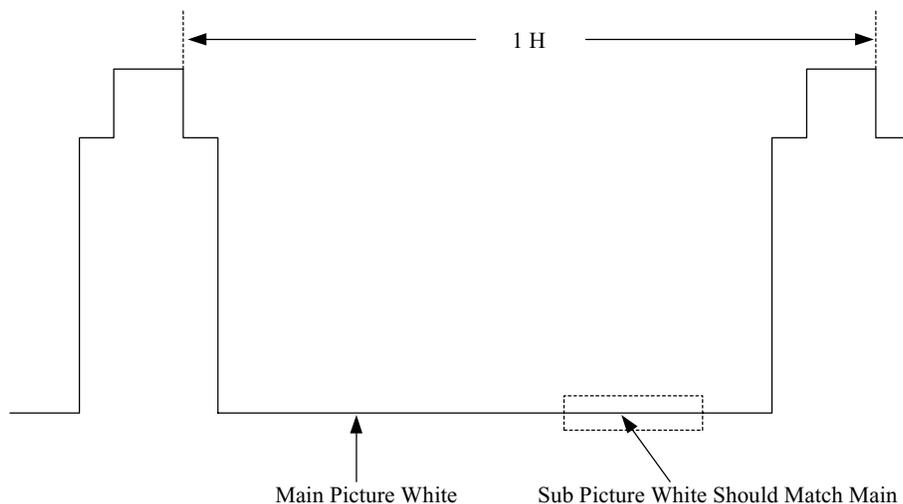
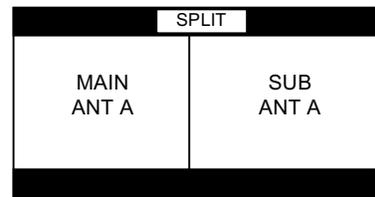
### Preparation for Adjustment   Adjustment Procedure

- |   |  |
|---|--|
| <p>[a] Sub Brightness adjustment should be finished.</p> <p>[b] Start adjustment 20 minutes after the power is turned on.</p> <p>[c] Condition should be set as follows:</p> <p>[d] Contrast = MAX</p> <p>[e] Brightness = Center</p> <p>[d] <b>PIP</b> mode should be in <b>SPLIT</b> mode.</p> <p>[e] Receive ANT A NTSC white signal, for the Main Picture and the Sub-Picture.</p> <p>[f] Connect Probe on the P852 (CRT PWB — Green) to check sub-picture amplitude.</p> | <ol style="list-style-type: none"> <li>1) Go to I<sup>2</sup>C adjustment Mode.</li> <li>2) Press “<b>MENU</b>” on remote to scroll through adjustment pages, until <b>TA1270-M</b> appears at the top of the page.</li> <li>3) Go to SUB CONT (TV-S)</li> <li>4) Press <b>PIP and PIP Mode</b> on remote control, TA1270-M changes to <b>TA1270-S</b>.</li> <li>5) Observe <b>P852</b> on the CRT PWB and change the TA1270-S “<b>SUB CNT</b>” I<sup>2</sup>C data so that the amplitude of the Sub Picture is the same level as that of the main picture. Shown below.</li> <li>6) Exit Service Menu.</li> </ol> |
|---|--|

Enter I<sup>2</sup>C adjustment Menu.  
Press Menu and scroll through pages until TA1270-M appears.

ADJUST MODE	
TA1270-M	
SUB CONT (TV-S)	**
OSD POSITION	<input type="checkbox"/>
AFC/CLOCK TEST	<input type="checkbox"/>
MEMORY INIT	<input type="checkbox"/>
I <sup>2</sup> COPEN	<input type="checkbox"/>
IR BLASTER	<input type="checkbox"/>

↓ Press PIP button and PIP Mode button.



Adjust SUB CONT (TV-S) until peak white of PinP matches peak white of the main picture.

## DP-2X HORIZONTAL POSITIONS (FINE) ADJUSTMENT

### Adjustment Preparation:

- Video Control: Brightness 90%,
- Contrast Max.

### Adjustment Procedure 16X9 Standard Mode:

- 1) Receive a 16X9 Standard crosshair signal.
- 2) Screen Format is NORMAL.
- 3) Enter the I<sup>2</sup>C Bus alignment menu and select Item [9] **H POSITION** and adjust the data so that the left and right sides are the same size.

- 4) Exit from the I<sup>2</sup>C Menu.

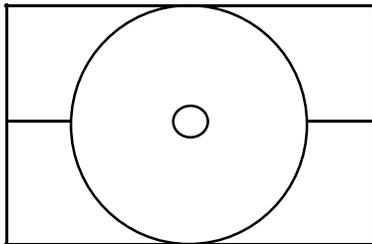
### 1080i 16X9 Standard Mode Adjustment:

- 5) Receive any 1080i (2.14H) signal.
- 6) Change Screen Format **16X9 Standard** mode.
- 7) Power the Set Off.
- 8) Enter the I<sup>2</sup>C Bus alignment menu and select Item [9] **H POSITION**
- 9) Adjust the data so that the left and right sides are the same size..
- 10)Exit from the I<sup>2</sup>C Menu.
- 11)Turn the Power Off.

***NOTE:** To enter the I<sup>2</sup>C Bus alignment menu, with Power Off, press the **INPUT** button and hold it down, then press the **POWER** button and release. I<sup>2</sup>C adjustment menu will appear.*

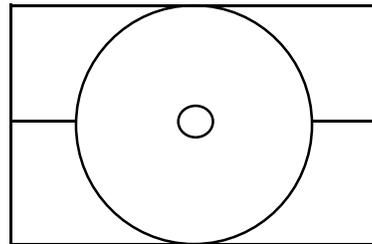
#### **16X9 NORMAL MODE:**

Balance left and right side display position.



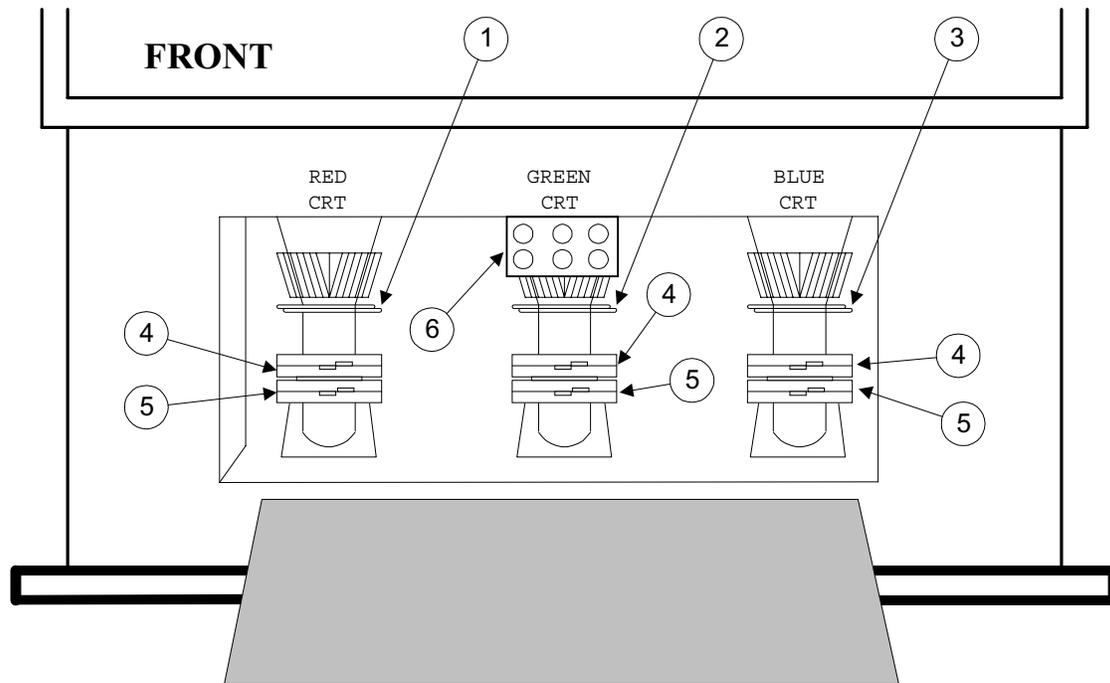
#### **1080i STANDARD MODE:**

Balance left and right side display position.



## DP-2X MAGNET AND YOKE LOCATION

### DP-2X MAGNETS Adjustment Points



- |                            |                            |
|----------------------------|----------------------------|
| (1) Centering magnet RED   | (5) Beam Alignment magnets |
| (2) Centering magnet GREEN | (6) Focus Block Assembly   |
| (3) Centering magnet BLUE  | RED, GREEN & BLUE          |
| (4) Beam Form Magnets      | FOCUS CONTROLS             |
|                            | Also: SCREEN CONTROLS      |
|                            | for RED, GREEN & BLUE      |

# **MISCELLANEOUS INFORMATION**

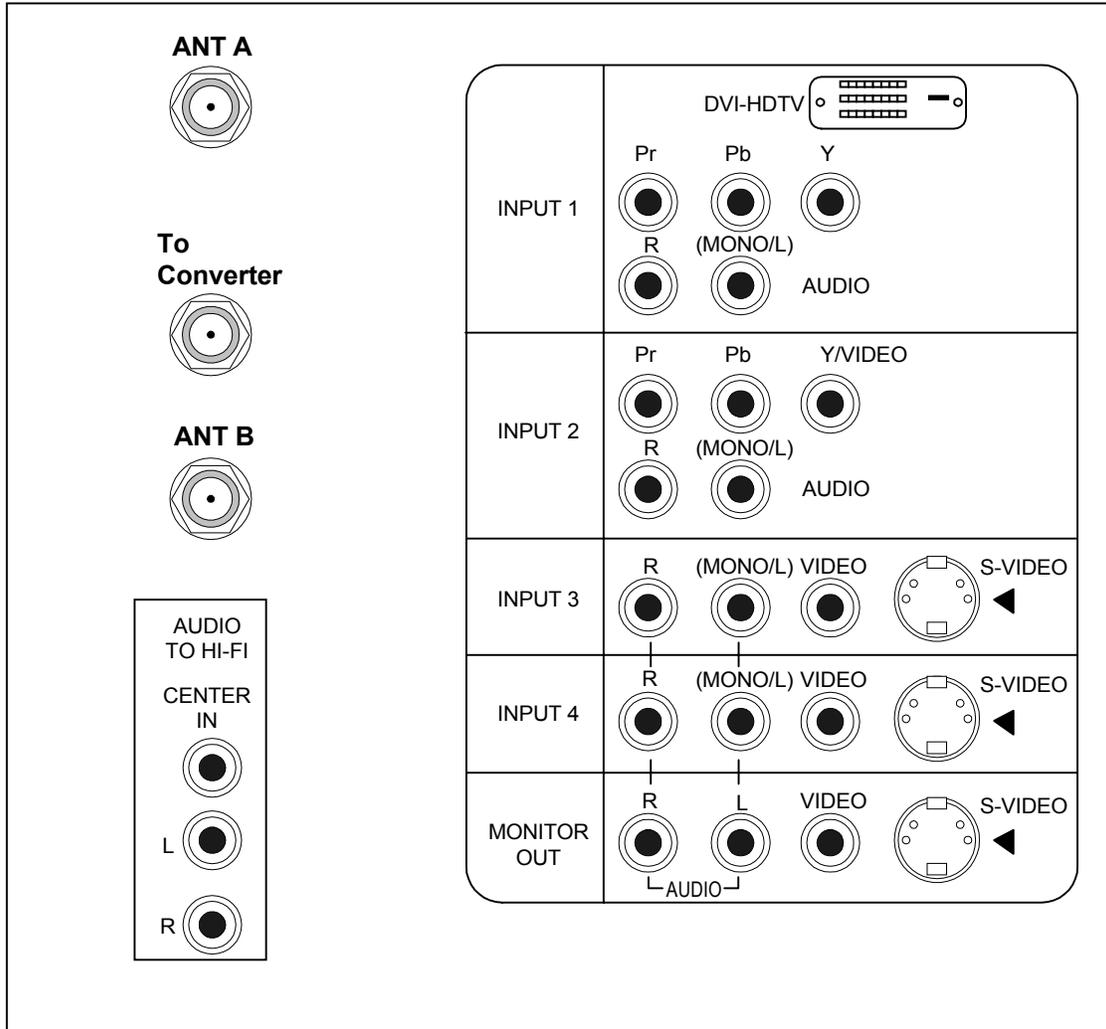
**DP-2X  
CHASSIS DIAGRAMS**

**SECTION 8**

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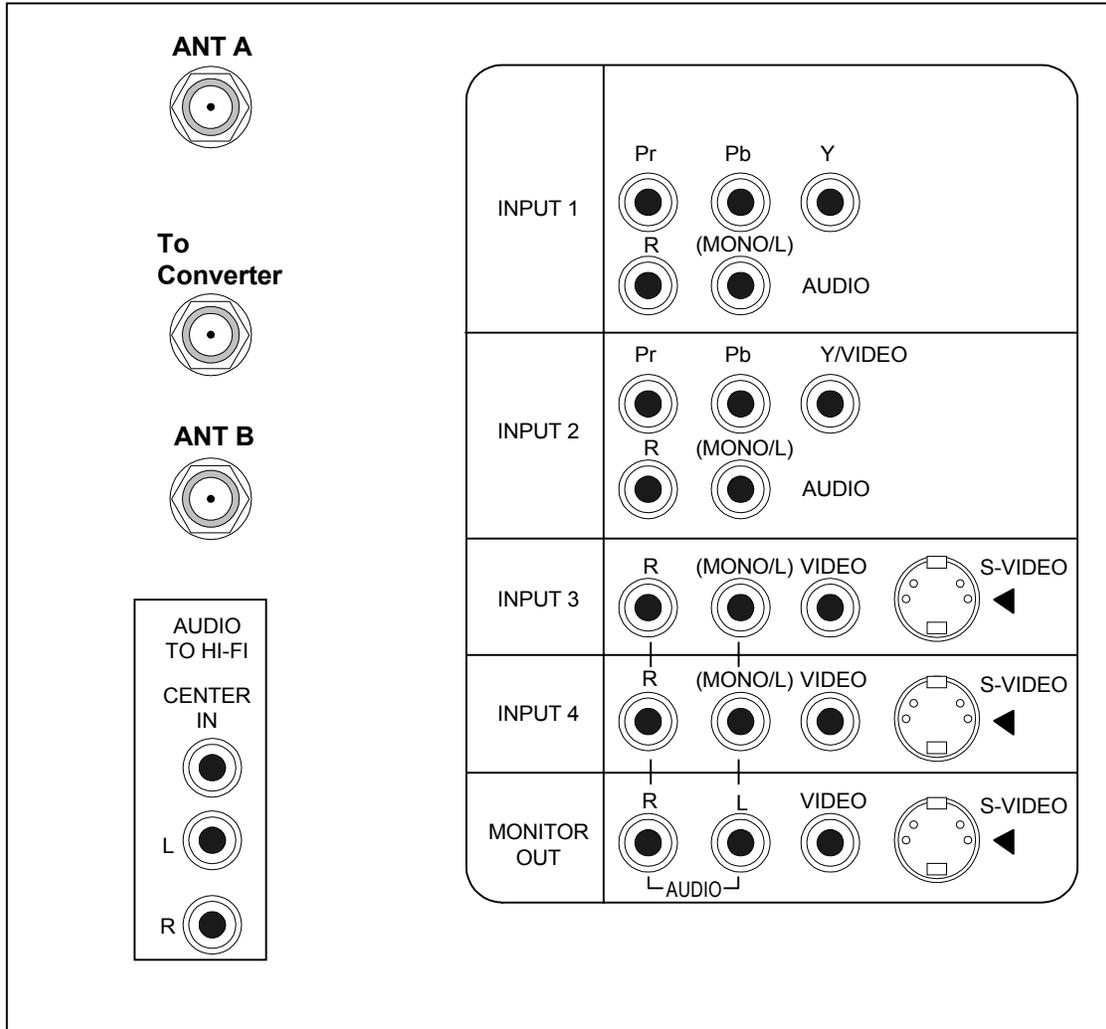
# DP-23 / 23G REAR PANEL

**51UWX20B, 57UWX20B DP-23 CHASSIS**  
**51GWX20B, 57GWX20B DP-23G CHASSIS**



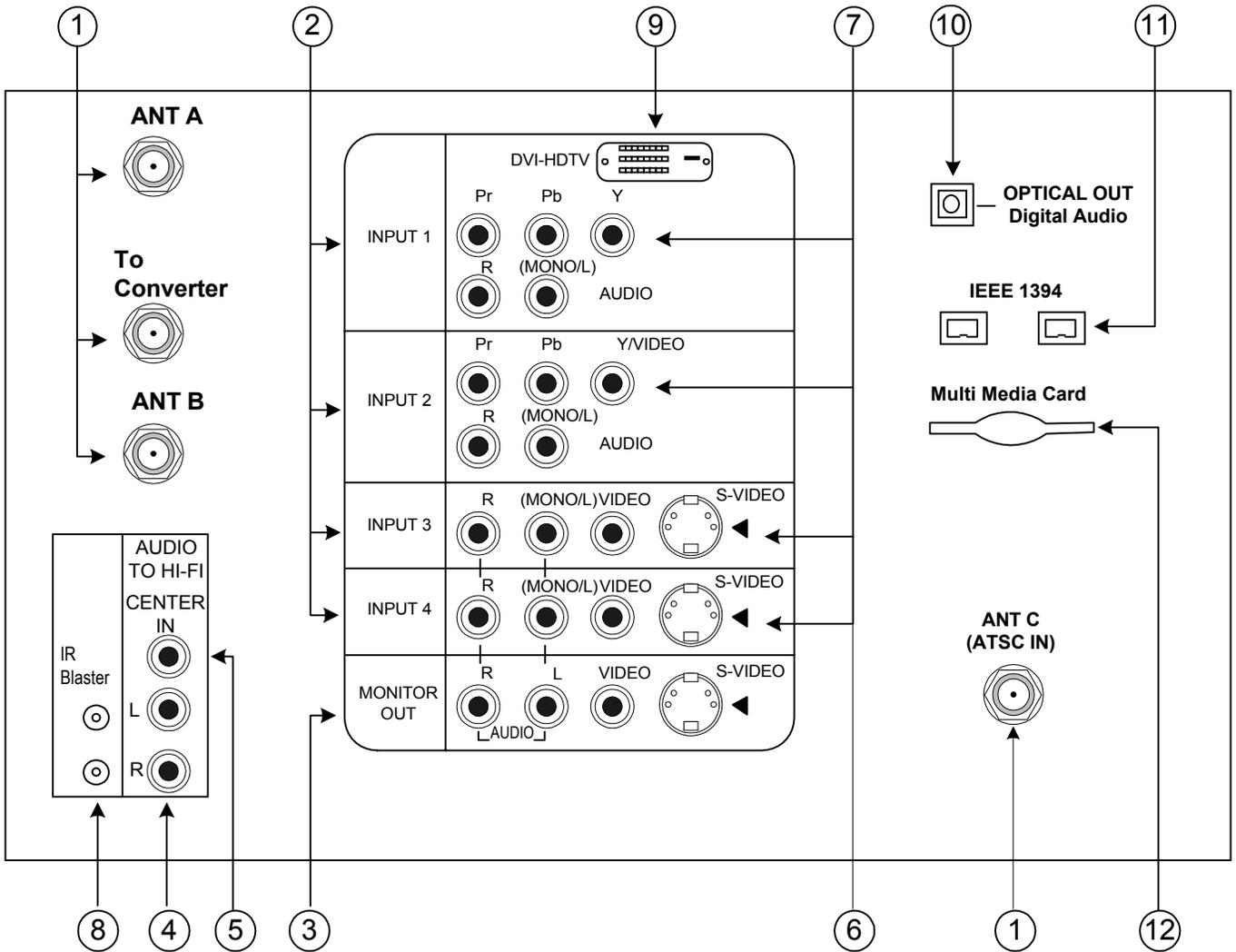
# DP-24 REAR PANEL

## 43FWX20B DP-24 CHASSIS



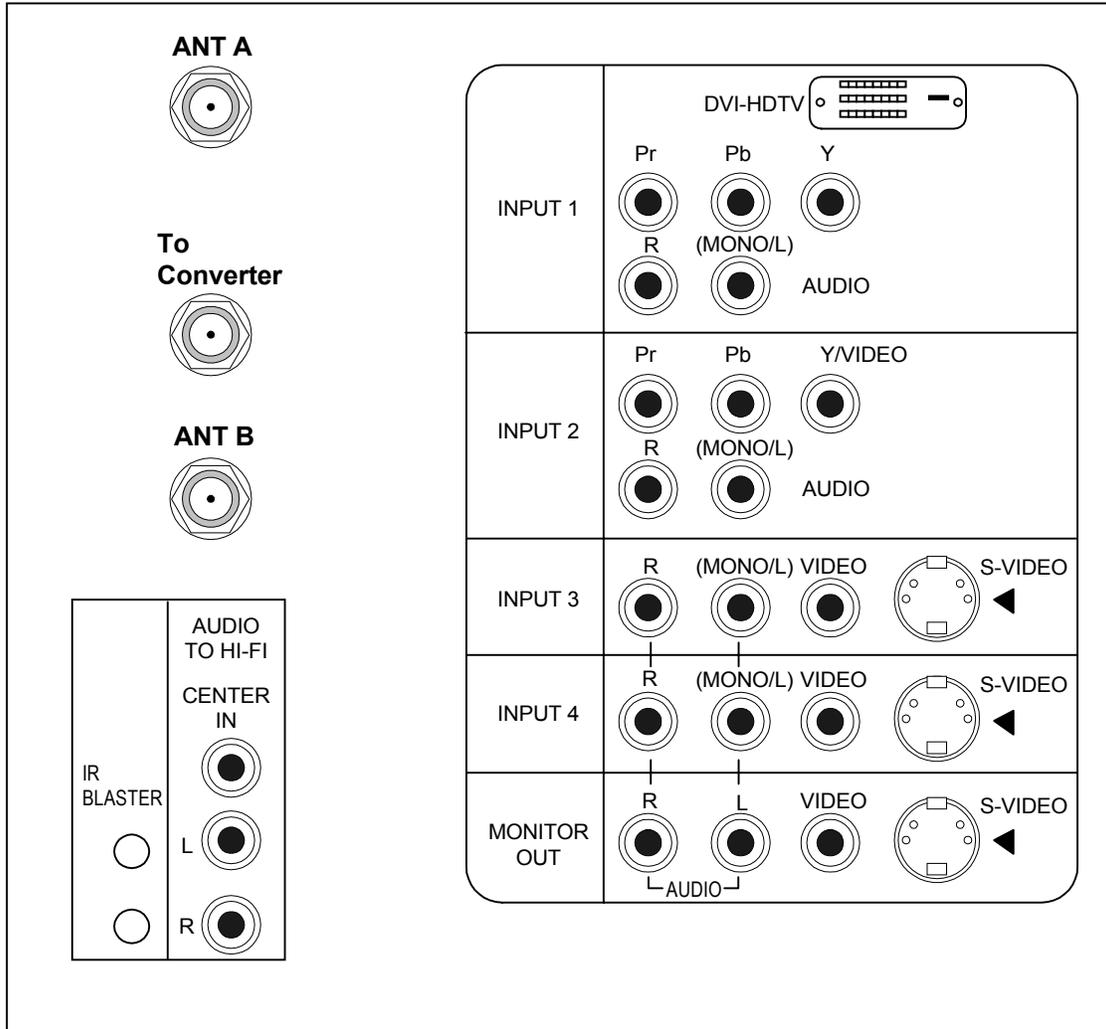
# DP-26 REAR PANEL

65XWX20B, 57XWX20B and 51XWX20B

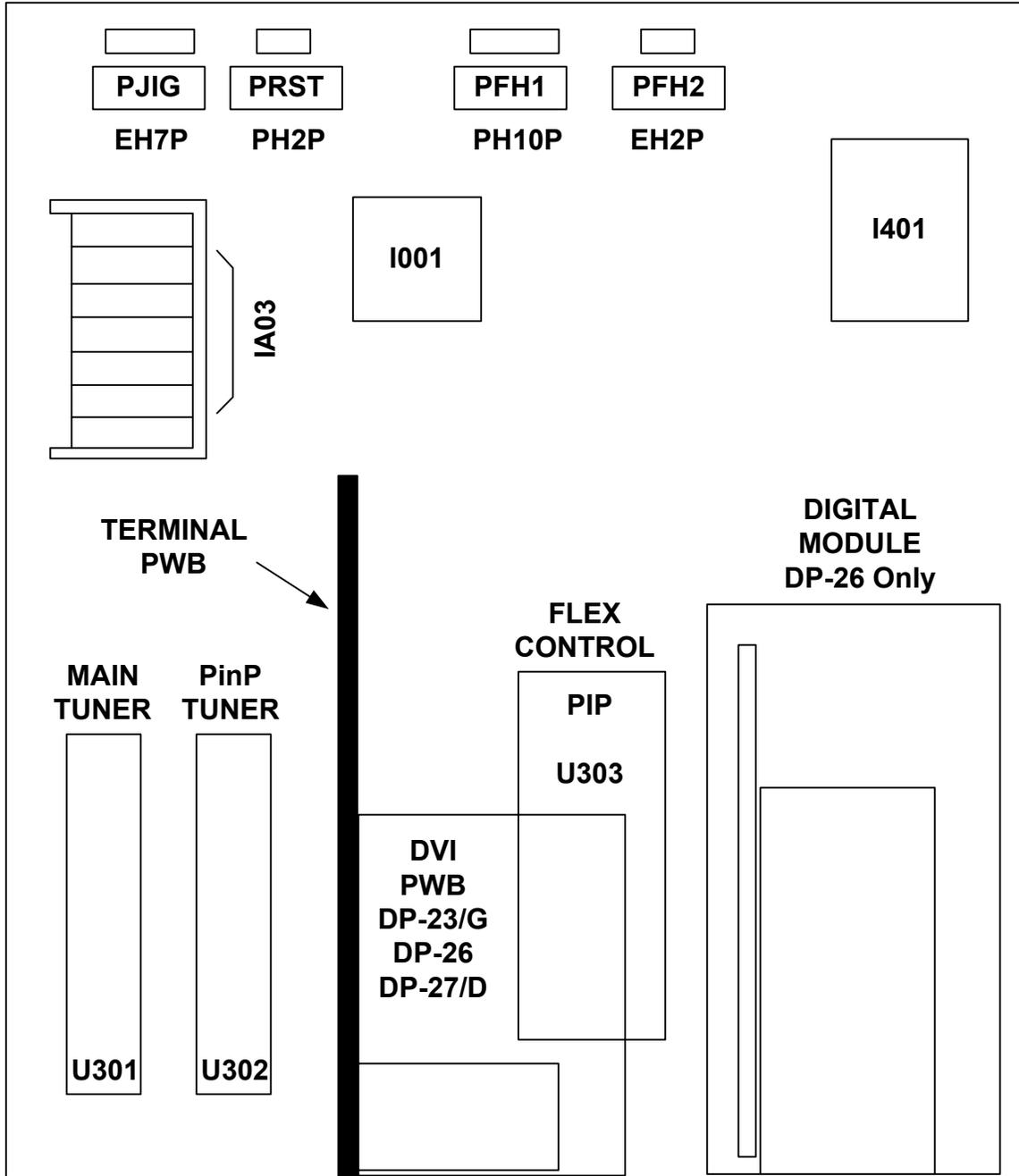


# DP-27 / 27D REAR PANEL

**51SWX20B, 57SWX20B, 65SWX20B DP-27 CHASSIS**  
**57TWX20B, 65TWX20B DP-27D CHASSIS**

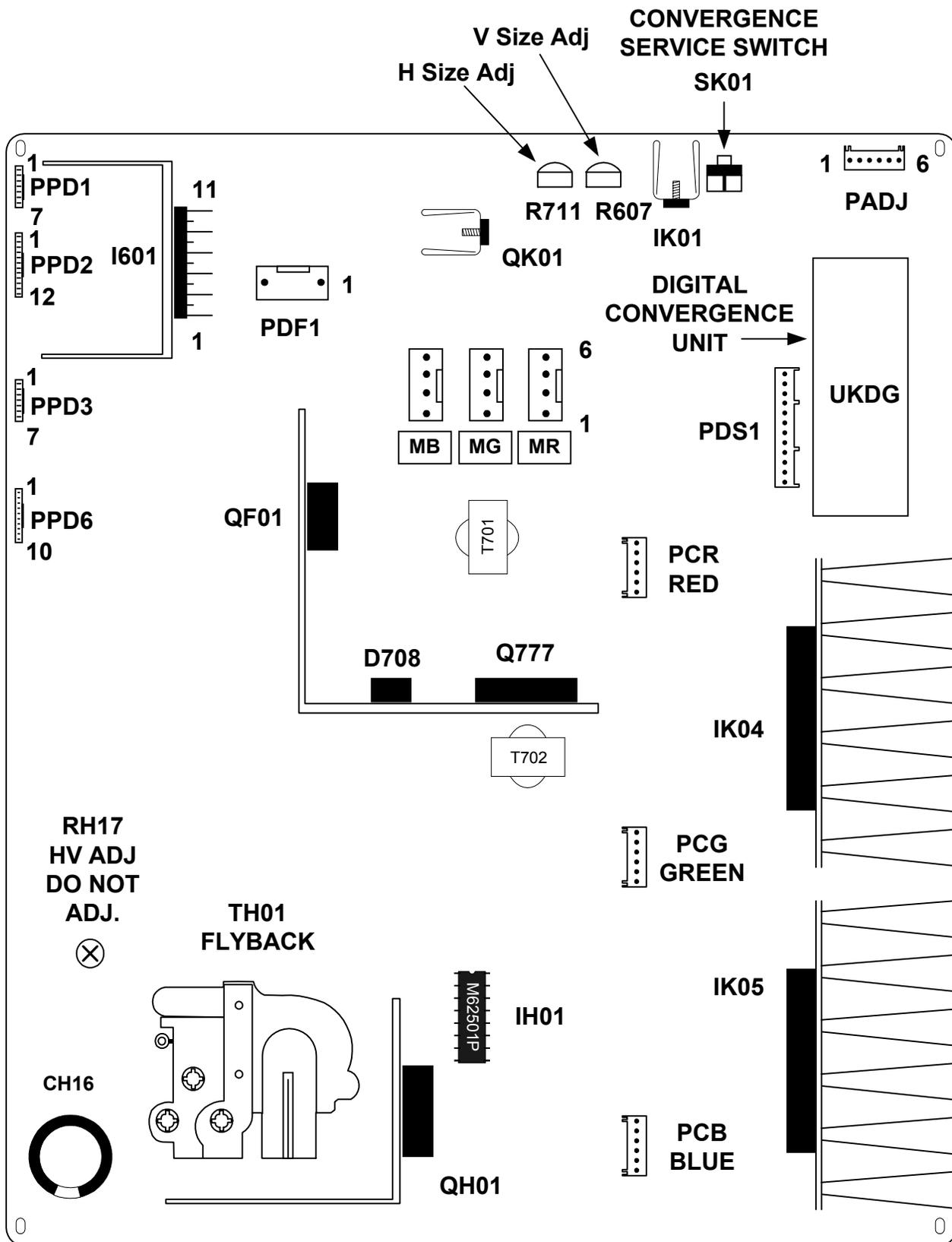


# DP-2X SIGNAL PWB

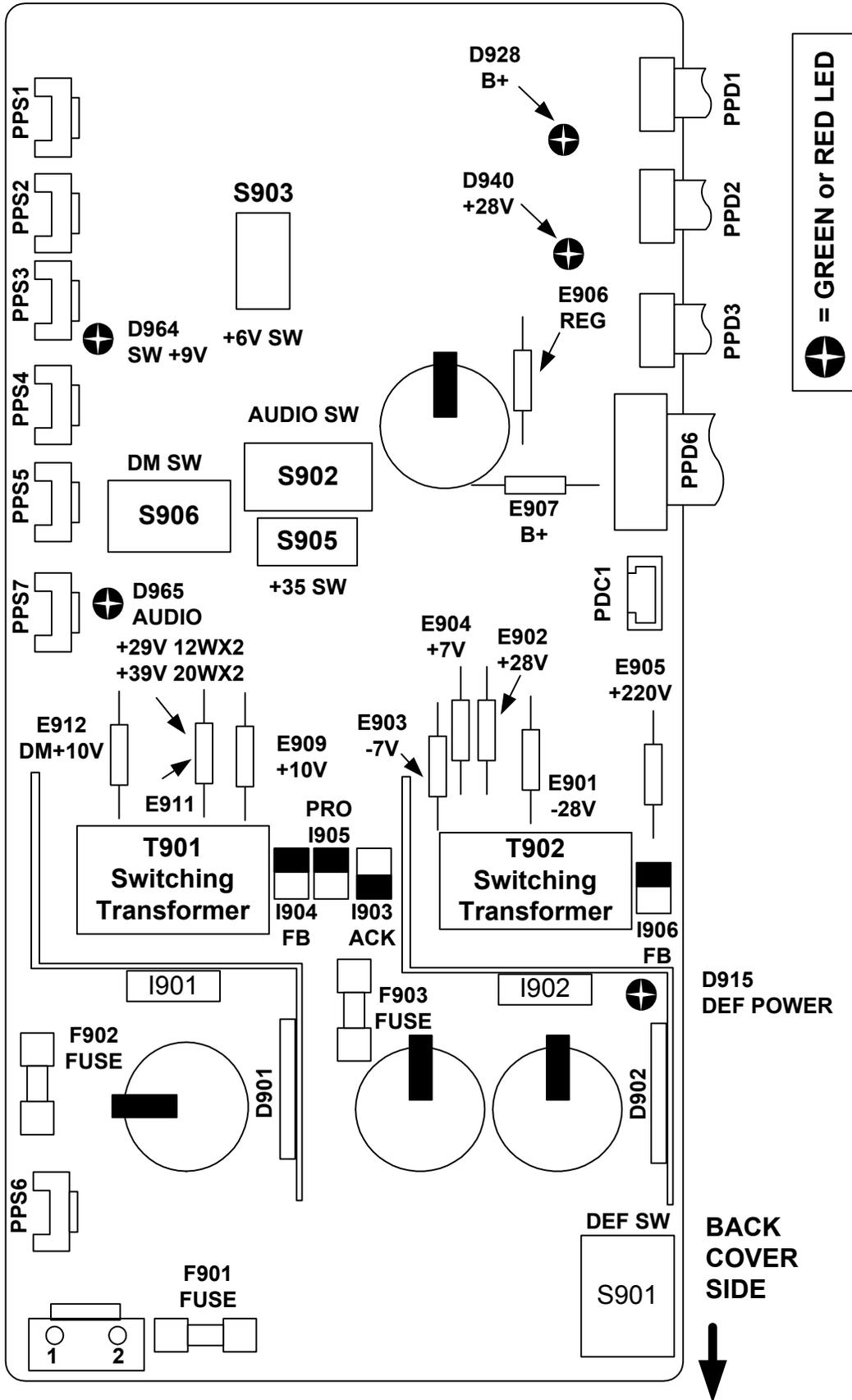


REAR  
VIEW

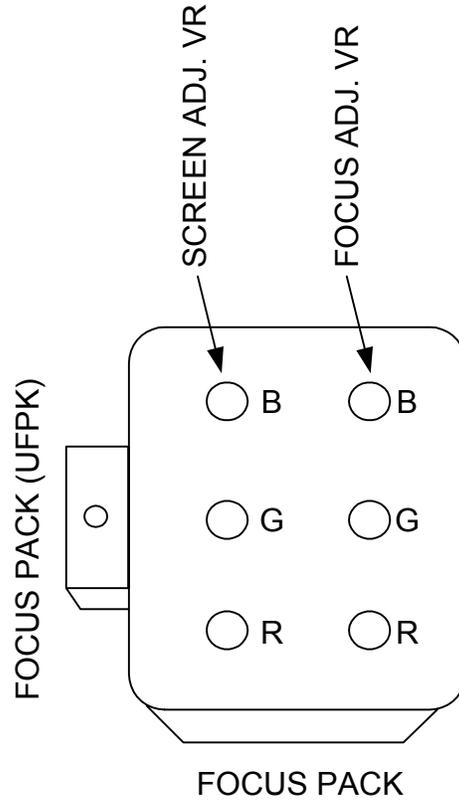
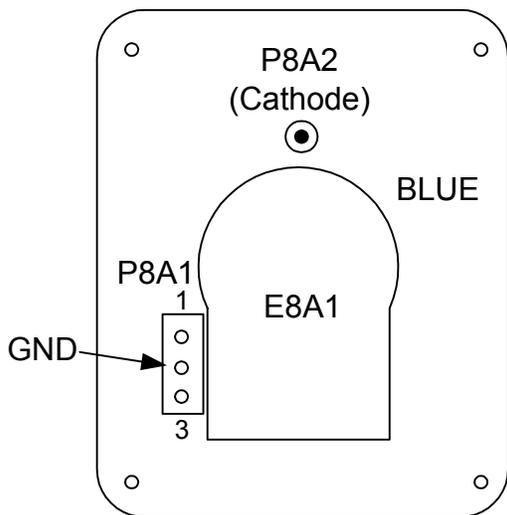
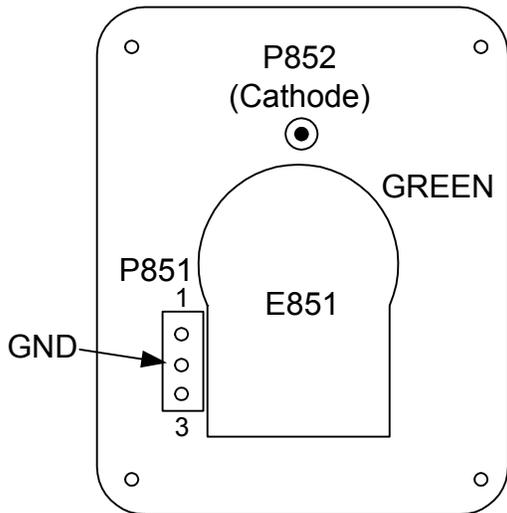
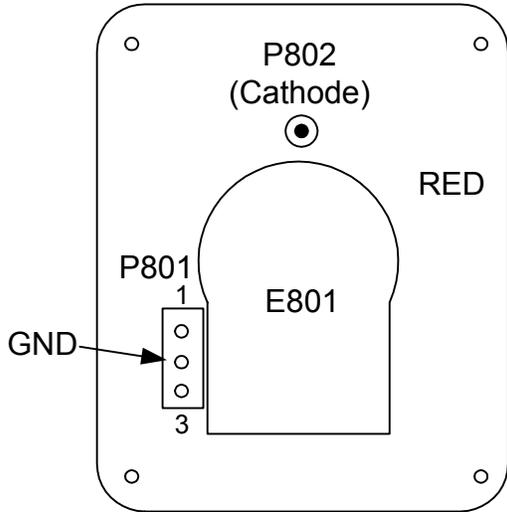
# DP-2X DEFLECTION PWB



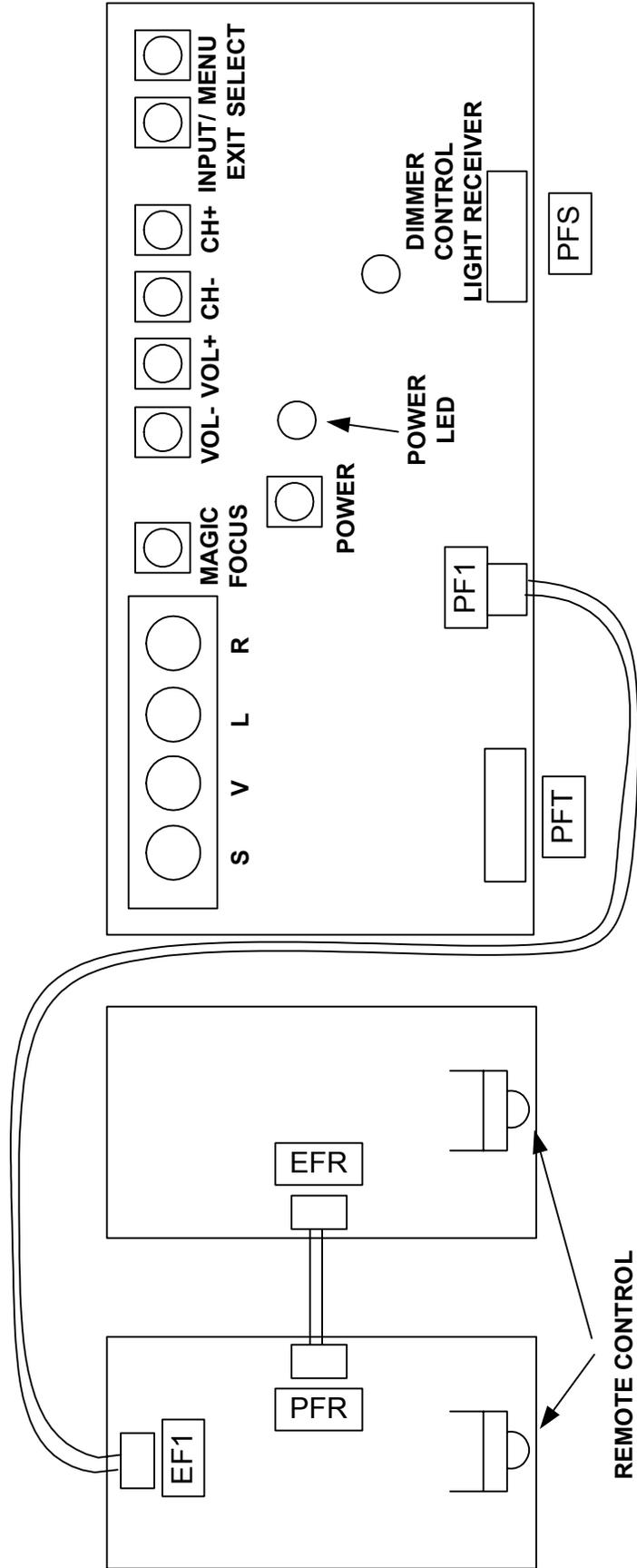
# DP-2X POWER SUPPLY PWB



# DP-2X CRT PWBs



# DP-X ALL BUT DP-24 FRONT CONTROL PWB



# DP-24 FRONT CONTROL PWB

